TAMPERE UNIVERSITY OF TECHNOLOGY

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DESIGN AND IMPLEMENTATION OF A BOOST-POWER-STAGE CONVERTER FOR PHOTOVOLTAIC APPLICATION

Master of Science Thesis

Examiner: Teuvo Suntio

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Aurinkopaneeli muuttaa auringosta tulevan sähkömagneettisen säteilyn sähköenergiaksi, joka voidaan siirtää sähköverkkoon tehoelektroniikan avulla. Aurinkopaneelin suurin lähtöteho, oikosulkuvirran arvo ja avoimen piirin jännite riippuvat ympäröivästä lämpötilasta ja säteilytehotiheyden arvosta. Niiden suurimmat mahdolliset arvot on tärkeää tietää suunniteltaessa aurinkopaneeliin kytkettyä hakkuriteholähdettä. Oikosulkuvirran ja avoimen piirin jännitteen suurimmat mahdolliset arvot saatiin selville ympärivuotisen säteilytehotiheyden ja lämpötilan mittaustiedon perusteella.

Tässä työssä suunniteltiin kaksi boost-tyyppistä hakkuriteholähdettä, joista ensimmäisen mitoitus perustui kirjallisuudessa esitettyyn menetelmään. Siinä kelan ja puolijohteiden mitoituksessa käytettävän virran arvo laskettiin jakamalla teholähteeseen syötetty teho sisäänmenojännitteen minimiarvolla. Toisen teholähteen mitoituksessa kelan ja puolijohteiden mitoituksessa käytettävän virran arvona käytettiin suoraan tietoa aurinkopaneelin suurimmasta mahdollisesta oikosulkuvirran arvosta.

Teholähteet suunniteltiin siten, että molemmissa on yhtä suuri kytkentätaajuinen tulojännitteen aaltoisuus ja kyky vaimentaa lähtöjännitteessä näkyvää matalataajuista aaltoisuutta siten, että se ei näkyisi tulojännitteessä. Vaikka teholähteet toimivat tältä osin sähköisesti samalla tavalla, ensimmäinen mitoitustapa johti suurempaan tulon kapasitanssiin ja suurempaan kelan sydämen kokoon sekä epätasaisempaan puolijohdekomponenttien lämpotilajakaumaan maksimitehpisteessä kuin jälkimmäinen mitoitustapa. Kirjallisuudessa esitetyllä mitoitustavalla päädytään siis ylimitoitukseen. Jos mitoitus tehdään tässä työssä esitellyllä uudella tavalla, voidaan saada aikaan huomattavia kustannussäästöjä varsinkin suuremmissa järjestelmissä, joissa tehot ovat suuria. Suunnitelluista teholähteistä rakennettiin prototyypit, joita mittaamalla edellä esitetyt tulokset varmennettiin.

ABSTRACT

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Photovoltaic generator is a device that converts solar radiation originated from the Sun into electrical energy. Power electronics are used to feed this electrical energy into the grid. In the design of a converter that is connected to the photovoltaic generator, it is important to know the maximum values of the generator output: Maximum output power, short-circuit current and open-circuit voltage, which are dependent on the amount of incident radiation and the value of ambient temperature. Maximum value for short-circuit current and open-circuit voltage were found based on the year-round irradiation and temperature measurement data.

In this thesis, two boost-power-stage converters were designed. Design of the first converter was based on the conventional method that was introduced in the literature. In that method, the inductor and semiconductors were sized by using current that was derived by dividing input power of the converter by input voltage. Value of the converter input power was calculated by multiplying the standard test condition output power of the selected photovoltaic generator by conventional sizing factor, which is the ratio of the converter nominal input power to the nominal output power of the photovoltaic generator. The second converter was designed by using the information about the real maximum output current of the selected photovoltaic generator, which is the short-circuit current.

The converters were designed in such a way that both have the same amount of switching frequency input voltage ripple and equal ability to prevent the low frequency output voltage ripple from affecting the input voltage. Even if the converters are electrically similar, the conventional design method leads to higher input capacitance, larger inductor core size and more uneven temperature distribution of the power semiconductors at the maximum power point than the new design method. Thus, the conventional design method leads to unnecessary oversizing. Significant cost savings can be achieved by applying the new design method, which is presented in this thesis for the first time. The results were verified by experimental measurements.

PREFACE

This Master of Science thesis was done for the Department of Electrical Engineering at Tampere University of Technology. The examiner of the thesis was Prof. Teuvo Suntio.

I want to express my gratitude to Prof. Teuvo Suntio for the interesting topic and guidance through the project. I also want to thank M.Sc. Tuomas Messo and M.Sc. Juha Jokipii for helping me with the converter model and with all kind of practical issues. Finally I want to thank the rest of the working group, especially M.Sc. Anssi Mäki for the information about the measurement system and the discussions about the properties of a photovoltaic generator.

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Jukka Viinamäki

CONTENTS

TERMS AND SYMBOLS

NOTATION

$\mathbf{A}$	System matrix
A_e	Cross-sectional area of the core
A_w	Cross-sectional area of the wire
a	Diode ideality factor
$\mathbf{B}$	Input matrix
$B_\mathrm{AC,PEAK}$	Peak value of alternating flux
B_max	Maximum flux density
$\mathbf{C}$	Output matrix
C	Capacitance
Δ	Characteristic polynomial
$\Delta i_\mathrm{L,pp}$	Inductor current peak-to-peak ripple
d	Duty ratio
d'	Complement of duty ratio
$\mathbf{D}$	Input-output matrix
D	Steady-state value of duty ratio
f_s	Switching frequency
G	Irradiance
G_n	Irradiance in standard test condition
G_a	Gain of pulse width modulator
G_c	Controller transfer function
$G_\mathrm{ci-o}$	Open-loop control-to-input transfer function
$G^\mathrm{S}_\mathrm{ci-o}$	Source-affected open-loop control-to-input transfer function
$G_\mathrm{co-o}$	Open-loop control-to-output transfer function
$G^\mathrm{S}_\mathrm{co-o}$	Source-affected open-loop control-to-output transfer function
G_ri	Reference-to-input transfer function
G_ro	Reference-to-output transfer function
$\mathbf{G}$	Matrix containing transfer functions of a converter
$G_\mathrm{io-o}$	Open-loop input-to-output transfer function
$G_\mathrm{io-\infty}$	Ideal forward current gain
$G_\mathrm{io\text{-}c}$	Closed-loop input-to-output transfer function
$G^\mathrm{S}_\mathrm{io\text{-}o}$	Source-affected input-to-output transfer function
H	Magnetic field strength
$I_\mathrm{d,rms}$	Root mean square of the diode current
i_in	Converter input current
i_o	Converter output current
$i_\mathrm{sc,n}$	Short-circuit current in standard test condition
$I_\mathrm{sw,rms}$	Root mean square of switch current
I_L	Steady-state value of inductor current
i_inS	Input current of non-ideal source
i_ph	Photocurrent
i_0	Saturation current
$I_\mathrm{L,p}$	Peak value of inductor current
$I_\mathrm{MPP,STC}$	Current in standard test condition
J	Flux density
K	Window utilization factor

l_{w}	Length of wire
m	Mass
$\mathbf{I}$	Identity matrix
k	Bolzmann constant
K_{I}	Temperature coefficient of short-circuit current
K_{V}	Temperature coefficient of open-circuit voltage
L	Inductance
L_{in}	Input voltage loop gain
l_{m}	Core magnetic path length
μ_0	Permeability of free space
μ_{e}	Core permeability
N	Number of turns
N_{s}	Number of series connected cells in a photovoltaic module
$P_{\mathrm{CU,DC}}$	Copper loss caused by direct current
P_{CORE}	Inductor core loss
$P_{\mathrm{d,cond}}$	Conduction loss of the diode
$P_{\mathrm{d,rev}}$	Power loss of the diode caused by reverse leakage current
$P_{\mathrm{d,tot}}$	Total power loss of the diode
$P_{\mathrm{MPP,STC}}$	Power in standard test condition
$P_{\mathrm{sw,c}}$	Conduction losses of power switch
$P_{\mathrm{sw,sw}}$	Switching losses of power switch
$P_{\mathrm{sw,tot}}$	Total power loss of power switch
P_{TOT}	Total power loss of inductor
q	Electron charge
R_{th}	Thermal resistance
$\mathbf{s}$	Laplace variable
T	Temperature
T_{s}	Switching period
$T_{\mathrm{oi-o}}$	Open-loop reverse voltage transfer ratio
$T_{\mathrm{oi-c}}$	Closed-loop reverse voltage transfer ratio
$T^{\mathrm{S}}_{\mathrm{oi-o}}$	Source-affected reverse voltage transfer ratio
$U_{\mathrm{MPP,STC}}$	Voltage in standard test condition
$u_{\mathrm{oc,n}}$	Open-circuit voltage in standard test condition
$WaAc$	Core area product
$\hat{x}$	AC-perturbation around a steady-state operation point
$Y_{\mathrm{o-o}}$	Open-loop output admittance
$Y_{\mathrm{o-c}}$	Closed-loop output admittance
$Y^{\mathrm{S}}_{\mathrm{o-o}}$	Source-affected output admittance
$Z_{\mathrm{in-o}}$	Open-loop input impedance
$Z_{\mathrm{in-c}}$	Closed-loop input impedance
$Z^{\mathrm{S}}_{\mathrm{in-o}}$	Source-affected input impedance
$Y_{\mathrm{o-}\infty}$	Ideal output admittance
Y_{S}	Output admittance of a non-ideal source
$Z_{\mathrm{in-oco}}$	Open circuit input impedance
$Z_{\mathrm{in-}\infty}$	Ideal input impedance

$Z_{\text{in}-\text{o}}$	Open-loop input impedance
$Z_{\text{in}-\text{c}}$	Closed-loop input impedance

ABBREVIATIONS

CC	Constant current
CCM	Continous conduction mode
CM	Conventional method
CF	Current-fed
CV	Constant voltage
CO_2	Carbon-dioxide
DC	Direct current
ESR	Equivalent series resistance
GM	Gain margin
MPP	Maximum power point
$MPPT$	Maximum power point tracking
NM	New method
OC	Open-circuit
PM	Phase margin
PV	Photovoltaic
PVG	Photovoltaic generator
PWM	Pulse width modulation
RMS	Root mean square
SC	Short-circuit
SF	Sizing factor

1. INTRODUCTION

Modern society is dependent on energy. Energy consumption is increasing mainly because of growing world population and improvement of our standard of living. In 2010, 87% of the total energy was produced from non-renewable fuels such as oil, coal and natural gas. About 6% was generated by nuclear power and the remaining 7% came from renewable resources such as hydro, biofuel, wind, solar and geothermal. With the present consumption, resources of non-renewable energy will run out in the near future. In addition, burning of fossil fuels generates pollutant gases such as CO_2, which is proved to be the main reason for the global warming problem. Long-term effect of global warming is very serious, since it will accelerate the gradual melting of the world's glaciers, which will increase the sea level. This has serious effect, since 100 million people live within 3ft above the sea water level. Global warmig will also cause damage to vegetation and agriculture because of droughts. Extreme weather conditions will happen more often and gulf stream might change substantially causing freezing weather in some parts of the world [1].

This trend could be affected by covering greater part of the energy production by renewable alternatives. It has been stated that 100% of the world's energy demand could be covered by hydro, wind and solar technologies [1]. Solar energy is one of the most promising alternatives, since it is abundantly available. Solar insolation could be used for heating but also conversion directly into electrical energy is possible using solar cells. A solar cell is a special kind of semiconductor diode, which causes DC current to flow when it is exposed to the light. Since the voltage of a single photovoltaic (PV) cell is low, a number of cells have to be connected together to form a PV module. Typical PV module includes tens of series connected PV cells. PV modules could be connected in series to form strings and parallel to form arrays and this kind of entity is generally called photovoltaic generator (PVG). Due to above mentioned reasons and because of decreased price of PV modules, the number of annual PV installations is increasing by the rate of 70%. As an example, installed annual global PV power reached about 30GW in 2011 [2].

Electrical energy that is produced by PVG can be fed into the grid or stored to an energy storage. This could be done by means of power electronics, which is important part of a PV power plant. As the amount of PV installations increases, it becomes more and more important to develop the power converters to be energy efficient, economical and reliable. All this means that the properties of the PVG should be taken into account when designing power converters for PV applications.

In a typical case of building the PV power plant, system integrator buys the PV modules and the power electronics from different manufacturers. Selection of the PV

generator is mainly based on the standard test condition (STC) power that the manufacturer provides in the datasheet. Power electronic devices are further selected based on the STC power of the PVG. In this stage, it is also checked that the maximum input current and maximum input voltage of the selected converter are high enough for the PVG. This leads to a situation, where the manufacturer of the converter would like to make it as universal as possible.

References [3] and [4] show explicitly that the component sizing of an interleaved-boost-power-stage for the PV application is based on the maximum input current that is calculated by dividing the input power of the converter by minimum input voltage. This sizing method leads to higher current than is possible to feed from the corresponding PV generator leading to oversizing. By inspecting the datasheets of the solar inverters, such a method seems to be commonly used [5],[6],[7]. These inverters are single-stage inverters where the level of the dc voltage is directly determined by the grid voltage. Therefore, the required dc voltage is much higher than defined in [3] and [4] leading to lower generator current.

The main goal of the thesis is to study how the PV generator affects the design of a power electronics converter connected directly to it. Two boost-power-stage DC/DC converters have been used as design example. One is designed based on the conventional design method and the other taking into account the special characteristics of a PV generator. The designs are done by using the same electrical characteristics in terms of input and output terminal ripple and power.

The rest of of the thesis is organized as follows: Chapter 2 presents the properties of a PVG and the limiting values for the terminal characteristics of the selected PV module are evaluated. Chapter 3 introduces the properties of a boost-power-stage converter in PV application and also the results of dynamic analysis are presented. Chapter 4 contains the complete design process starting from the specification and ending to the control design. Chapter 5 presents the measurements of the prototypes by illustrative graphs and the final chapter aggregates the most important results of the study.

2. PROPERTIES OF A PHOTOVOLTAIC MODULE

2.1 Modeling of a Photovoltaic Module

Electrical characteristics of an ideal PV cell can be represented by a parallel connection of a current source and a diode. The current source describes a photovoltaic current i_{ph}, which is directly proportional to the incident radiation and the diode represent the properties of a $p-n$ junction. Practical PV cells also contain losses, which are included in the model as shunt resistance r_{sh} and series resistance r_{s} as presented in Fig. 2.1. In Fig. 2.1, i_{d} is the diode current, u_{d} is the diode voltage, i_{sh} is the current through the shunt resistance, i_{pv} is the output current of the cell and u_{pv} is the terminal voltage of the PV cell [8].

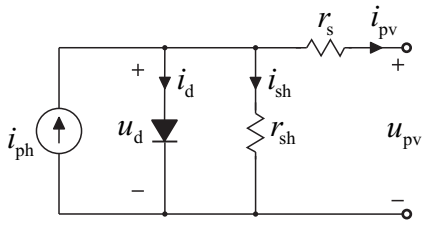


Figure 2.1: Single-diode model of a photovoltaic cell.

In addition to a single PV cell, single-diode model in Fig. 2.1 could also represent a PV module, which constitutes of several cells connected in series. Equation that mathematically describes the I-U characteristics of the practical PV module is presented in (2.1) [8].

$$i_{\mathrm{pv}} = i_{\mathrm{ph}} - i_0 \left[\exp\left(\frac{u_{\mathrm{pv}} + r_{\mathrm{s}} i_{\mathrm{pv}}}{N_{\mathrm{s}} a k T / q} \right) - 1 \right] - \frac{u_{\mathrm{pv}} + r_{\mathrm{s}} i_{\mathrm{pv}}}{r_{\mathrm{sh}}}, \tag{2.1}$$

where i_{ph} is the photocurrent generated by the incident light, i_0 is the saturation current, N_{s} is the number of series connected cells, a is the diode ideality factor, k is the Bolzmann constant, T is the temperature of the $p-n$ junction and q is the electron charge. More sophisticated models have been developed but the single-diode model offers good compromise between accuracy and complexity.

When the current i_{pv} is zero, PV cell is said to operate in open-circuit condition (OC). Respectively, when the voltage u_{pv} is zero, PV cell operate in short-circuit condition (SC). In both of these conditions, the output power of the PV cell is zero and the maximum output power is found to be in between of these conditions, which is

called the maximum power point (MPP).

Typical current-voltage (I-U) curve of a PV module, the output power and the dynamic resistance are presented with normalized values in Fig. 2.2. The dynamic resistance includes the effect of the diode, shunt resistance and series resistance. It represents the low-frequency value of the PV module output impedance and is defined as the slope $\Delta u_{\mathrm{pv}}/\Delta i_{\mathrm{pv}}$ of an I-U curve. As shown in Fig. 2.2, the dynamic resistance is non-linear and dependent on the operating point. [9]

The operating range between SC and MPP is called constant current (CC) region, since the output current is relatively constant and the value of the dynamic resistance is high. Respectively, the operating range between MPP and OC is called constant voltage (CV) region, since the output voltage stays relatively constant and the value of the dynamic resistance is rather low.

Output voltage of a PV module should be kept precisely at the MPP, since even a small change will decrease the output power. Maximum power point tracking (MPPT) algorithm is generally used in the converter to locate the MPP, since its location is affected by incident radiation and ambient temperature. Voltage ripple at the output of a PV module caused by power converter connected to it, might also cause significant decrease in energy yield. According to [10], the effect of voltage ripple on eneregy yield is even more severe in partial shading condition, when I-U curve is sharper. This means that the power converter connected to a PVG should be designed to have as small voltage ripple as possible.

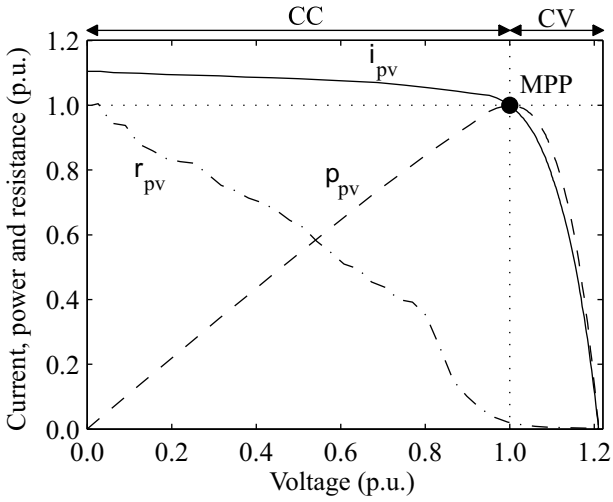


Figure 2.2: Typical I-U curve and dynamical resistance of a PV module.

Only electrical parameters that PV module manufacturers usually give in their datasheets are open-circuit voltage, short-circuit current, MPP voltage and power at the MPP. These values are measured in so called standard test condition (STC) of 1000W/m^2 solar irradiance, 25°C cell temperature and air mass (AM) of 1.5. Air mass means the mass of air between the PV module and the sun, which affects the spectral distribution and intensity of sunlight. Because of limited data from the manufacturer, the parameters in (2.1) have to be solved by other means.

The shunt resistance r_{sh} in Fig. 2.1 describes the leakage current of the $p-n$ junction and it depends on the fabrication method of the PV cell. Effect of the shunt resistance is stronger in the CC region. For rough estimation, it can be approximated to be infinite. The series resistance r_{s} represents the sum of different structural resistances within the PV module and its effect is strongest in the CV region. For a rough estimation, series resistance can be approximated to be zero. Since the series resistance is usually low compared to the parallel resistance, it is common to assume that short circuit current equals the photocurrent of the PVG (i.e. $i_{\mathrm{sc}} \approx i_{\mathrm{ph}}$). [8]

The photocurrent i_{ph} is linearly depenent on the solar irradiation and is also affected by ambient temperature according to (2.2).

$$i_{\mathrm{ph}} = \left(i_{\mathrm{ph,n}} + K_{\mathrm{I}}\Delta_{\mathrm{T}}\right)\frac{G}{G_{\mathrm{n}}}, \tag{2.2}$$

where $i_{\mathrm{ph,n}}$ is the photovoltaic current at the STC, K_{I} is the temperature coefficient, Δ_{T} is the difference between actual temperature and the temperature in STC, G is the actual irradiance on the surface of the PV module and G_{n} is the irradiance on the surface of the PV module in STC. Generally, the value of the temperature coefficient is low.

The value of the saturation current i_0 in (2.1) can be found using (2.3).

$$i_0 = i_{0,\mathrm{n}}\left(\frac{T_{\mathrm{n}}}{T}\right)^3 \exp\left[\frac{qE_{\mathrm{g}}}{ak}\left(\frac{1}{T_{\mathrm{n}}} - \frac{1}{T}\right)\right], \tag{2.3}$$

where T_{n} is the temperature of the $p-n$ junction in STC, T is the actual temperature, E_{g} is the bandgap energy of the semiconductor and $i_{0,\mathrm{n}}$ is the nominal saturation current, which can be expressed by

$$i_{0,\mathrm{n}} = \frac{i_{\mathrm{sc,n}}}{\exp\left(u_{\mathrm{oc,n}}q/N_{\mathrm{s}}akT_{\mathrm{n}}\right) - 1}, \tag{2.4}$$

where $i_{\mathrm{sc,n}}$ is the short circuit current and $u_{\mathrm{oc,n}}$ is the open circuit voltage both in the STC.

A simplified expression for the open-circuit voltage of the PV module is presented in (2.5). It is based on (2.1) and (2.2) assuming that $r_{\mathrm{s}} = 0$, $r_{\mathrm{sh}} \to \infty$, $i_{\mathrm{sc}} = i_{\mathrm{ph}}$, $K_{\mathrm{I}} = 0$ and by taking into account that in the open-circuit condition $i_{\mathrm{pv}} = 0$. By using (2.3), (2.4) and (2.5), the open-circuit voltage of the PV module can be estimated based on the ambient temperature, irradiance level and the aforementioned parameters given by the manufacturer.

$$u_{\mathrm{oc}} = \ln\left(\frac{Gi_{\mathrm{sc,n}}}{G_{\mathrm{n}}i_{\mathrm{o}}} + 1\right)\frac{N_{\mathrm{s}}akT}{q} \tag{2.5}$$

2.2 Effect of Climate Conditions on the PV Module

The simulated I-U curve of NAPS NP190Gkg PV module, which is used in this thesis, is shown in Fig. 2.3 at two different temperature and irradiance levels. The linear depency of the short-circuit current on irradiance level was expressed mathematically in (2.2) and it is also visible in this graph. The dashed curve crosses the y-axis almost at the same point as the solid line, which means that the effect of ambient temperature on short-circuit current is low, complying to the information given by (2.2). Respectively, the dashed and solid lines cross the x-asis as pairs, which means that the open-circuit voltage is affected more by ambient temperature than irradiance level.

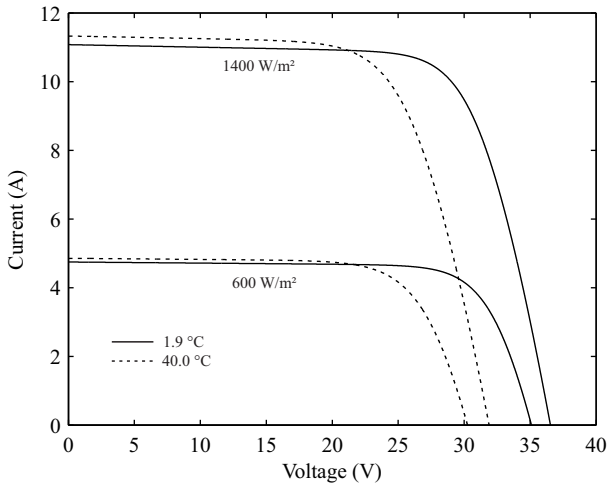


Figure 2.3: Simulated I-U curve of the NAPS NP190GKg PV module

According to Fig. 2.3 and Ref. [8], it is reasonable to assume that the effect of ambient temperature on short-circuit current is negligible. In this case, the short-circuit current of the PV panel is solely determined by incident radiation. Thus, the maximum value for the short-circuit current is found according to the maximum value of incident radiation.

When the sunlight passes through the atmosphere, a part of the radiation is absorbed and scattered. On a clear day approximately 75% of the solar irradiation coming from the sun passes through the atmosphere without scattering or absorbtion. This part of the irradiation is called direct irradiance. Some of the scattered sunlight is not scattered into space, but ends up on the surface of the earth. This part of the radiation is called diffuse radiation. Route of the scattered sunlight might be quite complicated. For example in snowy areas, sunlight might scatter first from the snow and then rescatter from the atmospere to the PVG. All of the scattered components are included in diffuse radiation. Sum of the direct irradiance and diffuse radiation is called global irradiance. [11]

Scattering of the sunlight from the edge of a cloud causes significant increase in diffuse radiation and further an increase in global radiation. This phenomenon is called the cloud enhancement. During the cloud enhancement, global radiation might

get higher than the average value of a solar radiation at the earth's surface which is 1000W/m^2.

Fig. 2.4 presents the global irradiance during the course of a day in July 2011. It is measured by using Kipp & Zonen SP lite2 pyranometer, which is located on the level and tilt angle corresponding to the PV modules. The measurement system and the PVG are on the rooftop of the Department of Electrical Engineering of Tampere University of Technology. The measurement data with a sampling interval of 100ms is stored on a server, which has been operating since 2011. According to the figure, solar irradiance can vary between 0%...130% of the average of 1000W/m^2. Thus, also short-circuit current of the PV module can vary between 0%...130% of the short-circuit current in STC.

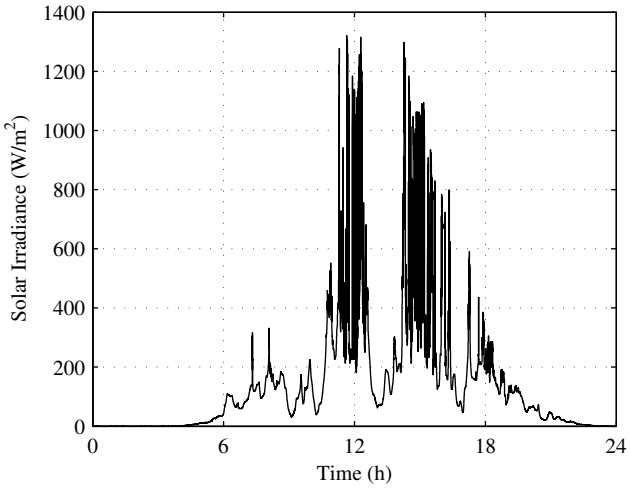


Figure 2.4: Measured irradiance on the surface of a PV module on 16$^{\text{th}}$ of July 2011.

Partial shading is a condition, where a part of the cells of a PVG are shaded. Typically trees, buildings and clouds cause partial shading. Also PV modules itself can cause partial shading to other PV modules in large PVG when the sun is in low position. Since the SC current of a PV cell is dependent on the irradiation level, it affects also the SC current of a sigle cell. If one of the series connected PV cells is shaded, the SC currents in other cells are higher than in the shaded cell. Shaded cell gets reverse biased if the current of the PV module is higher than the SC current of the shaded cell. This causes the shaded cell to act as a load and thus it disspipates part of the power generated by non shaded cells. If the output of the PV module is short-circuited during this kind of partial shading situation, all of the power generated in PV module will be dissipated in the shaded cell and damaging is most likely to happen. [12]

Hot spot heating during the partial shading can be avoided by connecting bypass diodes antiparallel with PV cells. It would be expensive to use a bypass diode for each cell, so usually one diode is used for groups of 12-24 cells. The bypass diode limits the negative voltage of a cell group to its treshold voltage (0.3 to 0.5 for Schottky diode) and enable the current to flow, thus decreasing the power dissipation. Shading of a

single cell causes the whole group to be bypassed meaning that also the non shaded cells in the group are bypassed and the output power of the PVG decreases by a large step. Thus, the group size is a tradeoff between price and sensivity to partial shading.[13]

2.3 Limit Values of NAPS NP190GKg PV Module Output

Maximum and minimum values of the current, voltage and power of the PV module output are needed in the design of a PV converter. The converter should be able to control its input voltage between the minimum and maximum MPP voltages of the PV module. Maximum value of the MPP voltage appears when the whole PV module is evenly illuminated and when the temperature is low and irradiance high. Respectively, the minimum value appears when the PV module is partially shaded so that only one group of the series connected cells is not bypassed and when the temperature is high and irradiance low.

The minimum and maximum values of NAPS NP190GKg PV module are of concern, since it is used in this thesis. Electrical characteristics of the module given in the manufacturer datasheet in STC are given in Table 2.1. These values are used in the calculations later on.

Table 2.1: Electrical characteristics of NAPS NP190GKg PV Module in STC

Parameter	Value
$U_{\mathrm{OC,STC}}$	33.1 V
$I_{\mathrm{SC,STC}}$	8.02 A
$P_{\mathrm{MPP,STC}}$	190 W
$U_{\mathrm{MPP,STC}}$	25.9 V
$I_{\mathrm{MPP,STC}}$	7.33 A

The internal connection of the PV cells inside NAPS NP190GKg PV module is presented in Fig. 2.5. The module consist of 54 series connected cells, which are divided into three groups, each of which has antiparallel bypass diode. These diodes are located in a module junction box.

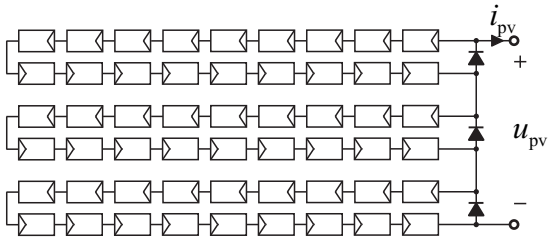


Figure 2.5: Internal connection of the PV cells inside NAPS NP190GKg PV module

The MPP voltage reaches its minimum value when two out of three of the bypass-diode groups are shaded. In this situation, current flows through two bypass diodes and 18 cells of non shaded group. Open-circuit voltage of a Si solar cell decreases by

rate of 2.3mV/K when temperature increases[13]. If the effect of irradiance on OC voltage is neglected, minimum MPP voltage $U_{\mathrm{MPP,MIN}}$ can be approximated by (2.6).

$$U_{\mathrm{MPP,MIN}} = \frac{U_{\mathrm{MPP,STC}} - (T_{\mathrm{MAX}} - T_{\mathrm{STC}})\, N_{\mathrm{s}} K_{\mathrm{V}}}{3} - 2U_{\mathrm{d}}, \tag{2.6}$$

where $U_{\mathrm{MPP,STC}}$ is the MPP voltage in STC, T_{MAX} is maximum cell temperature, T_{STC} is the cell temperature in STC, which is $25°C$, K_{V} is the temperature coefficient of the cell voltage and U_{d} is the forward voltage drop of the bypass diode. Minimum MPP voltage is 5.8 V, when the following values are used: $T_{\mathrm{MAX}} = 60°C$, $N_{\mathrm{s}} = 54$, $U_{\mathrm{d}} = 0.7V$. This value is used in Chapter 3 as the minimum input voltage of the converter.

Maximum output voltage of the PV module was found by substituting the measurement data of the irradiance and the backplate temperature of NAPS NP190GKg PV module to the simplified equation (2.5). The same measurement setup has been used here as it was used to produce Fig. 2.4. Temperature was measured by using PT100 temperature sensor located on the back of the PV module. It was predicted, that the maximum peak of the OC voltage would take place in the spring when temperature is low and a peak in diffuse radiation would be formed due to cloud enhancement.

By studying the measurement data from June 2011 to May 2012, it was observed that the highest peak in OC voltage and in glogal irradiance took place on 5$^{\mathrm{th}}$ of April 2012. Measured irradiance during the course of that day is shown in Fig. 2.6. As it is shown, the irradiance level fluctuates heavily and the peak takes place around noon, caused most likely by the cloud enhancement.

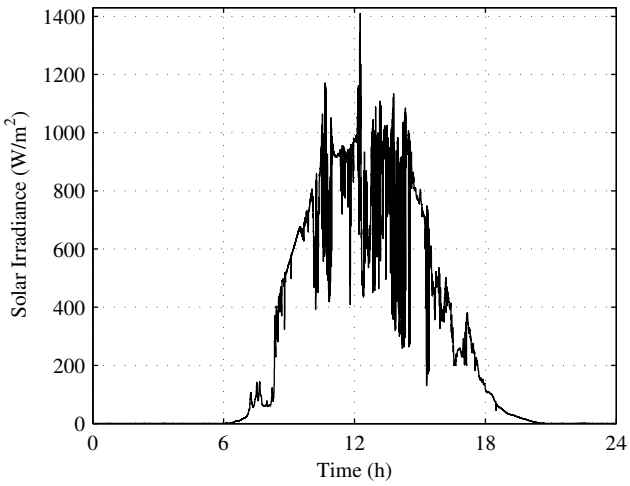


Figure 2.6: Measured irradiance on the surface of PV module on 5$^{\mathrm{th}}$ of April 2012.

An extended view of the global irradiance peak value is shown in Fig. 2.7. The irradiance level stays above 1000W/m^2 for several minutes, around 1300W/m^2 for a minute and around 1400W/m^2 for several seconds. Backplate temperature of NAPS NP190GKg PV module is presented in Fig. 2.8 measured at the same time as global

irradiance. Backplate temperature is quite low and increases slowly. Actually the temperature stays almost constant compared to irradiance during the measurement period.

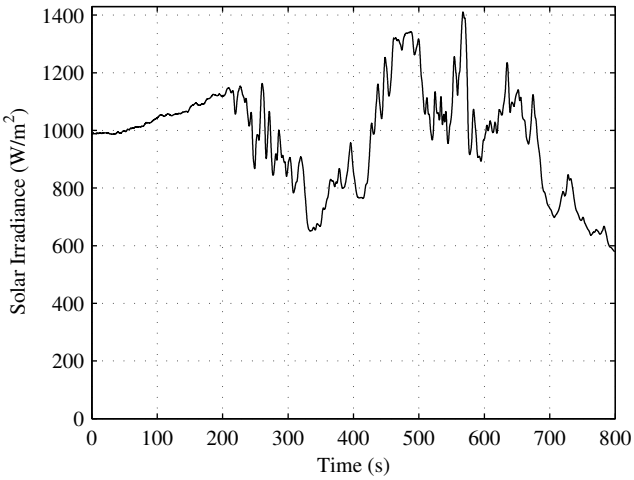


Figure 2.7: Measured peak in the irradiance on the surface of PV module during the cloud passing conditions.

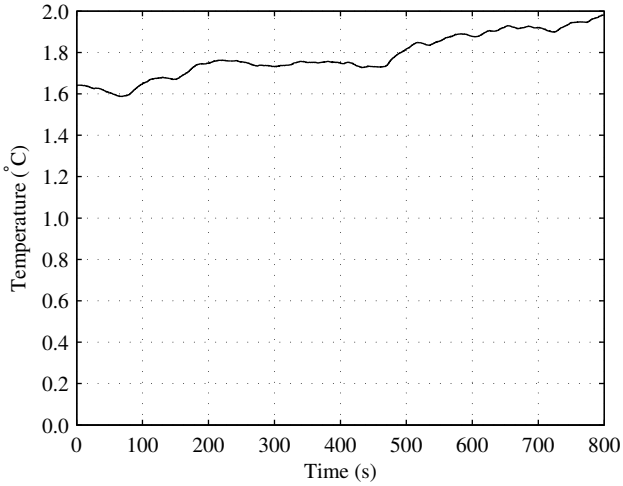


Figure 2.8: Measured temperature on the back of PV module during the cloud passing conditions.

Open-circuit voltage in Fig. 2.9 was calculated by substituting the data of Fig. 2.7 and Fig. 2.8 to equation (2.5). As it is shown, OC voltage stays around 35 V during the whole measurement period. Because this graph was achieved by the simplified model that neglects the effect of shunt and series resistance, the maximum OC voltage was also simulated by Matlab® Simulink model based on (2.1). This model is already verified to be valid for the same PV module in the prior research [12]. Temperature of 1.9°C and irradiance of 1400W/m^2 were used in the simulation. As it is visible in the simulated I-U curve of Fig. 2.10, maximum open-circuit voltage is 36.5V, which is one volt higher than the value achieved by the simplified model. Simulated value is

selected since it is obtained by more accurate model. SC current in the I-U curve of Fig. 2.10 is about 11A. This is in accordance with (2.2), which predicts that it is 1.4 times the SC current in STC when temperature depency is ignored.

Measured maximum value of 1400W/m^2 for the global irradiance is consistent with the prior research [14], in which it was mentioned that the global irradiance might be around 1000W/m^2 - 1500W/m^2 with the duration of 20s to 140s. This obviously depends on the location of the PVG. Similarly, the maximum OC voltage of the PV module is heavily dependent on the location. For example if the ambient temperature is always high, OC voltage will not achieve high value even if the irradiance is high.

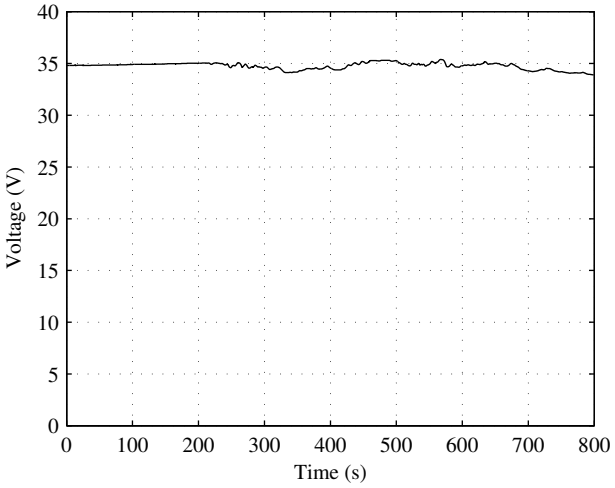


Figure 2.9: Calculated open-circuit voltage of NAPS NP190GKg PV module based on measured irradiance and temperature data during the cloud passing conditions.

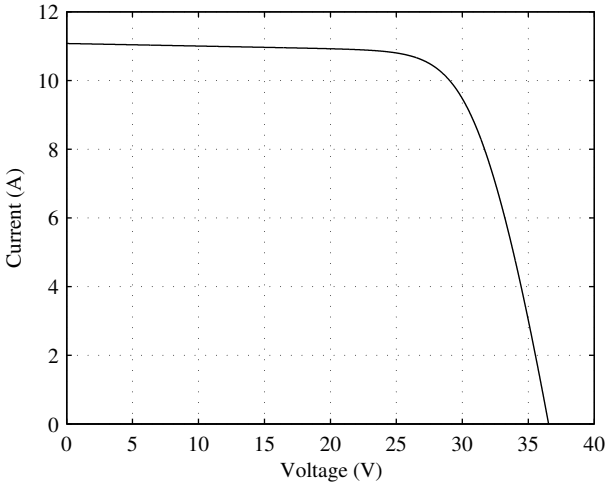


Figure 2.10: Simulated I-U curve of NAPS NP190GKg PV module in maximum open-circuit voltage condition.

3. OPERATION OF A BOOST-POWER-STAGE CONVERTER

In the grid connected solar energy systems, one common approach is to use double-stage conversion, in which there is the single-phase or three-phase inverter after the boost-power stage converter. In this way, greater variances in input voltage can be tolerated and the maximum input voltage can be smaller compared to the single-stage conversion consisting only the inverter [13]. It is also possible that the losses caused by partial shading are smaller due to less series connected PV modules [12].

Other benefits of the boost topology in photovoltaic applications are that the input current is continuous and that blocking diode is included in the topology so no additional diode is needed. Blocking diode is needed to prevent current from flowing back to the PVG during the night or other times of low irradiation. [15]

The maximum power point tracking is carried out in the DC/DC converter and the DC/AC converter controls its output current and input voltage as the grid connection requires. The DC/DC converter can operate at open or closed loop. In the open loop operation, duty ratio is directly controlled by MPPT. In the closed loop operation, MPPT-algorithm calculates the input voltage reference, which is then used as a reference value for the closed loop controller of the converter. The block diagram of the double-stage inverter is presented in Fig. 3.1 [16]

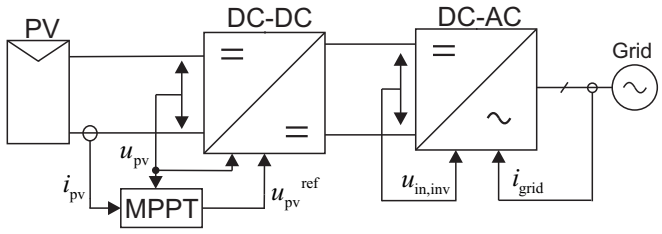


Figure 3.1: Double-Stage Inverter [16].

In this thesis, the DC/DC converter of the double-stage conversion scheme is implemented by taking into account that it is a part of the double-stage inverter presented above. This means that the effects of PVG and inverter on the dynamics of the DC/DC converter are taken into account. Closed-loop control scheme is used and the reference value for the controlled variable is provided manually, which means that the MPP tracking is not implemented.

Controlling of the input-side variable is compulsory for maximizing power transfer [17]. Output current of the PVG is directly proportional to the irradiance, which varies in large scale and fast. Controlling of the PVG output current thus requires fast

dynamics to follow the MPP and it could easily lead to saturation of the controller. On the other hand, the change in irradiance only slightly affects on the output voltage of the PVG. Instead, it is directly proportional on the temperature, which has slow dynamics and hence the output voltage control of the PVG is preferred. [15]

Based on this information, input-voltage-based feeback control is implemented in the DC/DC converter. As inverter controls its input voltage, it behaves as a voltage type load for the DC/DC converter. This means that the DC/DC converter in this application should be considered as current-fed current output(CF-CO) converter.

The main circuit diagram of the converter is given in Fig. 3.2. It can be obtained by adding a capacitor to the input of a conventional boost converter in a similar manner as it has been done for the buck converter in [18].

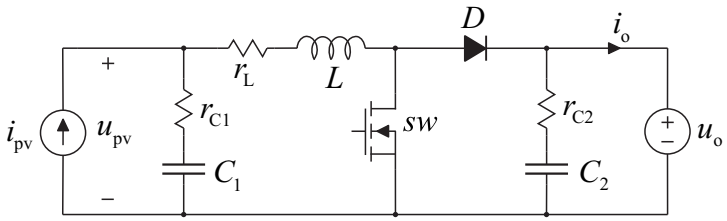


Figure 3.2: Power-stage of a current-fed dc-dc converter.

3.1 Dynamic Modeling

The frequency-domain (i.e. small-signal) model of the boost-power-stage converter is created in this thesis in order to the facilitate control design and to find out optimal value of the input capacitor C_1 in Fig. 3.2. The small-signal model of the converter describes the relation between input and output variables of the system. As it is shown in Fig. 3.2, the input current and output voltage of the converter are determined externally and so they are input variables of the system. Input voltage and output current of the converter can be affected by controlling the duty ratio, so they are the output variables of the system. Since the input voltage is to be controlled, the relation between the control variable and the input voltage is the most interesting from the control design point of view.

Both of the converters designed in this thesis operate in continuous conduction mode (CCM), which means that the inductor current is either rising or falling but it never reaches zero. This means that the main circuit diagram in Fig. 3.2 is divided into two subcircuits: The on-time subcircuit when the switch is conducting and the inductor current is rising and the off-time subcircuit when the switch is not conducting and the inductor current is falling. Based on the on-time and off-time subcircuits and by following the procedure presented in [19], the linearized state-space model (3.1) of the converter was obtained. The merged resistance R_{eq} and voltage U_{eq} in (3.1) are defined in 3.2.

$$
\begin{aligned}
\frac{\mathrm{d}\hat{i}_\mathrm{L}}{\mathrm{d}t} &= -\frac{R_\mathrm{eq}}{L}\hat{i}_\mathrm{L} + \frac{1}{L}\hat{u}_\mathrm{C1} + \frac{r_\mathrm{C1}}{L}\hat{i}_\mathrm{in} - \frac{D'}{L}\hat{u}_\mathrm{o} + \frac{U_\mathrm{eq}}{L}\hat{d} \\
\frac{\mathrm{d}\hat{u}_\mathrm{C1}}{\mathrm{d}t} &= -\frac{1}{C_1}\hat{i}_\mathrm{L} + \frac{1}{C_1}\hat{i}_\mathrm{in} \\
\frac{\mathrm{d}\hat{u}_\mathrm{C2}}{\mathrm{d}t} &= -\frac{1}{r_\mathrm{C2}C_2}\hat{u}_\mathrm{C2} + \frac{1}{r_\mathrm{C2}C_2}\hat{u}_\mathrm{o} \\
\hat{u}_\mathrm{in} &= -r_\mathrm{C1}\hat{i}_\mathrm{L} + \hat{u}_\mathrm{C1} + r_\mathrm{C1}\hat{i}_\mathrm{in} \\
\hat{i}_\mathrm{o} &= D'\hat{i}_\mathrm{L} + \frac{1}{r_\mathrm{c2}}\hat{u}_\mathrm{C2} - \frac{1}{r_\mathrm{C2}}\hat{u}_\mathrm{o} - I_\mathrm{in}\hat{d},
\end{aligned}
\tag{3.1}
$$

$$
\begin{aligned}
R_\mathrm{eq} &= r_\mathrm{C1} + r_\mathrm{L} + Dr_\mathrm{SW} + D'r_\mathrm{D} \\
U_\mathrm{eq} &= \left[r_\mathrm{D} - r_\mathrm{SW}\right] I_\mathrm{in} + U_\mathrm{o} + U_\mathrm{D},
\end{aligned}
\tag{3.2}
$$

The linearized state-space model in (3.1) can also be presented in the matrix form as in (3.3) and (3.4).

$$
\begin{bmatrix} \frac{\mathrm{d}\hat{i}_\mathrm{L}}{\mathrm{d}t} \\ \frac{\mathrm{d}\hat{u}_\mathrm{C1}}{\mathrm{d}t} \\ \frac{\mathrm{d}\hat{u}_\mathrm{C2}}{\mathrm{d}t} \end{bmatrix} = \begin{bmatrix} -\frac{R_\mathrm{eq}}{L} & \frac{1}{L} & 0 \\ -\frac{1}{C_1} & 0 & 0 \\ 0 & 0 & -\frac{1}{r_\mathrm{C2}C_2} \end{bmatrix} \begin{bmatrix} \hat{i}_\mathrm{L} \\ \hat{u}_\mathrm{C1} \\ \hat{u}_\mathrm{C2} \end{bmatrix} + \begin{bmatrix} \frac{r_\mathrm{C1}}{L} & -\frac{D'}{L} & \frac{U_\mathrm{eq}}{L} \\ \frac{1}{C_1} & 0 & 0 \\ 0 & \frac{1}{r_\mathrm{C2}C_2} & 0 \end{bmatrix} \begin{bmatrix} \hat{i}_\mathrm{in} \\ \hat{u}_\mathrm{o} \\ \hat{d} \end{bmatrix} \tag{3.3}
$$

$$
\begin{bmatrix} \hat{u}_\mathrm{in} \\ \hat{i}_\mathrm{o} \end{bmatrix} = \begin{bmatrix} -r_\mathrm{C1} & 1 & 0 \\ D' & 0 & \frac{1}{r_\mathrm{c2}} \end{bmatrix} \begin{bmatrix} \hat{i}_\mathrm{L} \\ \hat{u}_\mathrm{C1} \\ \hat{u}_\mathrm{C2} \end{bmatrix} + \begin{bmatrix} r_\mathrm{C1} & 0 & 0 \\ 0 & -\frac{1}{r_\mathrm{C2}} & -I_\mathrm{in} \end{bmatrix} \begin{bmatrix} \hat{i}_\mathrm{in} \\ \hat{u}_\mathrm{o} \\ \hat{d} \end{bmatrix} \tag{3.4}
$$

Linearized state-space in (3.3) and (3.4) is now in the standard state-space form as given in (3.5). Inductor current and capacitor voltages are state variables, input current, duty ratio and output voltage are the input variables as well as input voltage and output current are output variables, respectively. The standard linearized state-space representation (3.5) can be transformed in to the frequency domain by Laplace transform, which yields (3.6).

$$
\begin{aligned}
\frac{\mathrm{d}\hat{\boldsymbol{u}}(t)}{\mathrm{d}t} &= \mathbf{A}\hat{\boldsymbol{x}}(t) + \mathbf{B}\hat{\boldsymbol{u}}(t) \\
\hat{\boldsymbol{y}}(t) &= \mathbf{C}\hat{\boldsymbol{x}}(t) + \mathbf{D}\hat{\boldsymbol{u}}(t)
\end{aligned}
\tag{3.5}
$$

$$
\begin{aligned}
s\boldsymbol{X}(s) &= \mathbf{A}\boldsymbol{X}(s) + \mathbf{B}\boldsymbol{U}(s) \\
\boldsymbol{Y}(s) &= \mathbf{C}\boldsymbol{X}(s) + \mathbf{D}\boldsymbol{U}(s)
\end{aligned}
\tag{3.6}
$$

Solving the relation between input and output variables from (3.6) yields

$$\boldsymbol{Y}(s) = (\mathbf{C}(s\mathbf{I} - \mathbf{A})^{-1}\mathbf{B} + \mathbf{D})\boldsymbol{U}(s) = \mathbf{G}\boldsymbol{U}(s), \tag{3.7}$$

Matrix $\mathbf{G}$ in (3.7) contains the transfer functions of the converter. Thus, (3.7) describes how to calculate the transfer functions when linearized state-space matrices are solved. Transfer function set of the boost-power-stage converter are as given in 3.8.

$$\begin{bmatrix} \hat{u}_{\text{in}} \\ \hat{i}_{\text{o}} \end{bmatrix} = \begin{bmatrix} Z_{\text{in-o}} & T_{\text{oi-o}} & G_{\text{ci-o}} \\ G_{\text{io-o}} & -Y_{\text{o-o}} & G_{\text{co-o}} \end{bmatrix} \begin{bmatrix} \hat{i}_{\text{in}} \\ \hat{u}_{\text{o}} \\ \hat{d} \end{bmatrix} \tag{3.8}$$

The ransfer function set (3.8) can be equally represented by linear two-port model as shown inside the dotted line in Fig. 3.3.

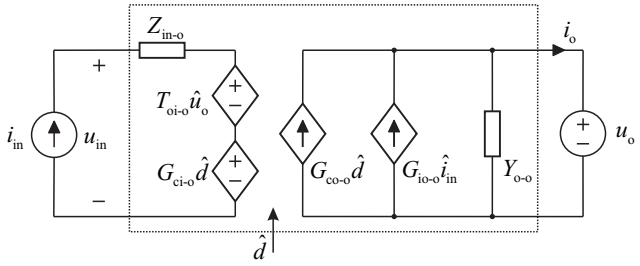


Figure 3.3: Linear two-port model of CF-CO converter.

The transfer functions in (3.8) were solved numerically by using Matlab® and used in the control design. The dynamical model of the boost-power-stage converter was constructed in [20] by analysing the CL-filter in the input side and PWM shunt regulator in the output side of the converter seperately and by merging them together. However, the resulting transfer functions of the converter are the same in [20] as in this thesis. The symbolically expressed open-loop transfer functions of the converter given in [20] are as follows:

$$
\begin{aligned}
Z_{\text{in-o}} &= \frac{1}{LC_1}\left(R_{\text{eq}} - r_{\text{C1}} + sL\right)\left(1 + sr_{\text{C1}}C_1\right)\frac{1}{\Delta} \\
T_{\text{oi-o}} &= \frac{D'}{LC_1}\left(1 + sr_{\text{C1}}C_1\right)\frac{1}{\Delta} \\
G_{\text{ci-o}} &= -\frac{U_{\text{eq}}}{LC_1}\left(1 + sr_{\text{C1}}C_1\right)\frac{1}{\Delta} \\
G_{\text{io-o}} &= -\frac{D'}{LC_1}\left(1 + sr_{\text{C1}}C_1\right)\frac{1}{\Delta} \\
G_{\text{co-o}} &= -I_{\text{in}}\left(s^2 - s\left(\frac{D'U_{\text{eq}}}{LI_{\text{in}}} - \frac{R_{\text{eq}}}{L}\right) + \frac{1}{LC_1}\right)\frac{1}{\Delta} \\
Y_{\text{o-o}} &= \frac{D^{\text{'2}}}{L}\cdot\frac{s}{s^2 + s\frac{R_{\text{eq}}}{L} + \frac{1}{LC_1}} + \frac{sC_2}{1 + sr_{\text{C2}}C_2},
\end{aligned}
\tag{3.9}
$$

where

$$
\Delta = s^2 + s\frac{R_{\text{eq}}}{L} + \frac{1}{LC_1}, \tag{3.10}
$$

Steady-state duty cycle D of the converter is as given in (3.11).

$$
D = \frac{\left(r_{\text{L}} + r_{\text{D}}\right)I_{\text{in}} - U_{\text{in}} + U_{\text{o}} + U_{\text{D}}}{\left(r_{\text{D}} - r_{\text{SW}}\right)I_{\text{in}} + U_{\text{o}} + U_{\text{D}}}, \tag{3.11}
$$

The closed-loop transfer functions of the input-voltage-controlled converter were also solved in [20] based on the control-block diagrams in Fig. 3.4 and Fig. 3.5 and are as follows

$$
\begin{aligned}
Z_{\text{in-c}} &= \frac{\hat{u}_{\text{in}}}{\hat{i}_{\text{in}}} = \frac{Z_{\text{in-o}}}{1 - L_{\text{in}}} \\
T_{\text{oi-c}} &= \frac{\hat{u}_{\text{in}}}{\hat{u}_{\text{o}}} = \frac{T_{\text{oi-o}}}{1 - L_{\text{in}}} \\
G_{\text{ri}} &= \frac{\hat{u}_{\text{in}}}{\hat{u}_{\text{in}}^{\text{ref}}} = -\frac{L_{\text{in}}}{1 - L_{\text{in}}}\cdot\frac{1}{G_{\text{se-in}}} \\
G_{\text{io-c}} &= \frac{\hat{i}_{\text{o}}}{\hat{i}_{\text{in}}} = \frac{G_{\text{io-o}}}{1 - L_{\text{in}}} - \frac{L_{\text{in}}}{1 - L_{\text{in}}}G_{\text{io-}\infty} \\
Y_{\text{o-c}} &= \frac{\hat{i}_{\text{o}}}{\hat{u}_{\text{o}}} = \frac{Y_{\text{o-o}}}{1 - L_{\text{in}}} - \frac{L_{\text{in}}}{1 - L_{\text{in}}}Y_{\text{o-}\infty} \\
G_{\text{ro}} &= \frac{\hat{i}_{\text{o}}}{\hat{u}_{\text{in}}^{\text{ref}}} = -\frac{L_{\text{in}}}{1 - L_{\text{in}}}\cdot\frac{G_{\text{co-o}}}{G_{\text{ci-o}}}\cdot\frac{1}{G_{\text{se-in}}},
\end{aligned}
\tag{3.12}
$$

where

$$
\begin{aligned}
&L_{\text{in}} = G_{\text{se-in}} G_{\text{c}} G_{\text{a}} G_{\text{ci-o}}, \\
&G_{\text{io-}\infty} = G_{\text{io-o}} - \frac{Z_{\text{in-o}} G_{\text{co-o}}}{G_{\text{ci-o}}}, \quad Y_{\text{o-}\infty} = Y_{\text{o-o}} + \frac{T_{\text{oi-o}} G_{\text{co-o}}}{G_{\text{ci-o}}},
\end{aligned}
\tag{3.13}
$$

where L_{in} is called input-voltage loop gain, $G_{\text{se-in}}$ is the input-voltage sensing gain, G_{c} is the input-voltage controller transfer function, G_{a} is the modulator gain, $G_{\text{io-}\infty}$ is ideal forward current gain and $Y_{\text{o-}\infty}$ is the ideal output admittance, respectively.

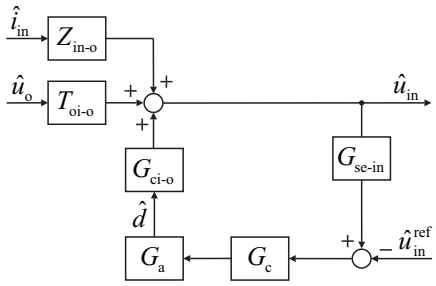


Figure 3.4: Control-block diagram of input dynamics [20].

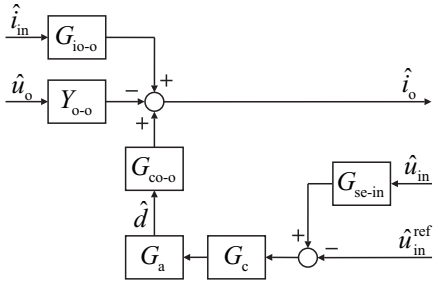


Figure 3.5: Control-block diagram of output dynamics [20].

Output power of a single-phase inverter fluctuates at twice the grid fequency, which causes a ripple component at the input voltage of the inverter. The requency of the ripple is also twice the grid frequency which is assumed to be 100 Hz in this thesis. If this ripple voltage ends up to the input side of the dc-dc converter, the voltage of the PV module will fluctuate around MPP reducing the energy yield.

Prevention of the output power fluctuation from affecting the input power is called power decoupling. Common power decoupling method is to add large capacitor parallel to the PV module or to the output of the DC/DC converter. Greatest drawback in this method is that the high-capacitance electrolytic capacitors, which are typically used, have limited lifetime and high price. Also various more complicated methods to implement power decoupling in the PV application are presented in the literature [21].

Transfer function $T_{\text{oi-c}}$ describes the relation between input and output voltages of the converter meaning that if $T_{\text{oi-c}}$ is smaller than unity, the converter will prevent output voltage ripple from affecting the input voltage. According to (3.12), $T_{\text{oi-c}}$ depends on the loop gain meaning that it can be affected by controller design. The higher

the controller gain, the greater the attenuation. Thus, the controller design should be implemented so that the loop gain is high enough at the frequency of 100 Hz. Small input capacitor can be used if the fluctuating power is handeled by the capacitor in the output of the dc-dc converter. The value of the output capacitor can be lower because the ripple in the output can be higher due to the attenuation of the converter. Great benefit is also that no additional components are needed as in some of the presented methods in [21].

3.2 The Effect of Nonideal Source

The closed-loop transfer functions of the converter in (3.9) were calculated by assuming that the source and load are ideal. However, PVG is not ideal and thus its effect on the converter dynamics shall be taken into account. Nonideal source can be modelled by adding admittance Y_S parallel to the input current source as shown in Fig. 3.6.

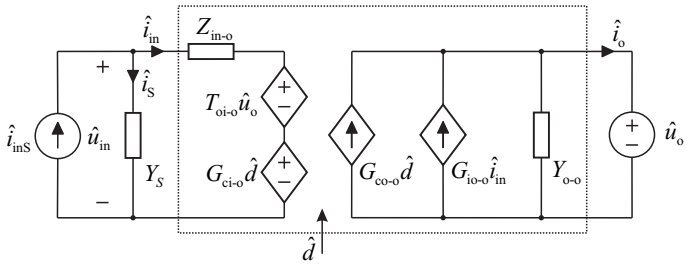


Figure 3.6: Linear two-port model of CF-CO converter with nonideal source.

Now, the input current of the converter is the input current i_inS subtracted by the current through the admittance i_S. When this new input current is substituted to (3.8), the source affected transfer functions of the converter (3.14) can be solved as instructed in [20].

$$\begin{bmatrix} \hat{u}_\mathrm{in} \\ \hat{i}_\mathrm{o} \end{bmatrix} = \begin{bmatrix} Z^\mathrm{S}_\mathrm{in\text{-}o} & T^\mathrm{S}_\mathrm{oi\text{-}o} & G^\mathrm{S}_\mathrm{ci\text{-}o} \\ G^\mathrm{S}_\mathrm{io\text{-}o} & -Y^\mathrm{S}_\mathrm{o\text{-}o} & G^\mathrm{S}_\mathrm{co\text{-}o} \end{bmatrix} \begin{bmatrix} \hat{i}_\mathrm{inS} \\ \hat{u}_\mathrm{o} \\ \hat{d} \end{bmatrix}$$
$$= \begin{bmatrix} \dfrac{Z_\mathrm{in\text{-}o}}{1+Y_\mathrm{s}Z_\mathrm{in\text{-}o}} & \dfrac{T_\mathrm{oi\text{-}o}}{1+Y_\mathrm{s}Z_\mathrm{in\text{-}o}} & \dfrac{G_\mathrm{ci\text{-}o}}{1+Y_\mathrm{s}Z_\mathrm{in\text{-}o}} \\ \dfrac{G_\mathrm{io\text{-}o}}{1+Y_\mathrm{s}Z_\mathrm{in\text{-}o}} & -\dfrac{1+Y_\mathrm{s}Z_\mathrm{in\text{-}oco}}{1+Y_\mathrm{s}Z_\mathrm{in\text{-}o}}Y_\mathrm{o\text{-}o} & \dfrac{1+Y_\mathrm{s}Z_\mathrm{in\text{-}\infty}}{1+Y_\mathrm{s}Z_\mathrm{in\text{-}o}}G_\mathrm{co\text{-}o} \end{bmatrix} \begin{bmatrix} \hat{i}_\mathrm{inS} \\ \hat{u}_\mathrm{o} \\ \hat{d} \end{bmatrix} \tag{3.14}$$

where $Z_\mathrm{in\text{-}oco}$ denotes the input impedance of the converter when the output of the converter is open-circuited and $Z_\mathrm{in-\infty}$ denotes the so called ideal input impedance given in Equations (3.15) and (3.16), respectively.

$$Z_\mathrm{in\text{-}oco} = Z_\mathrm{in} + \frac{G_\mathrm{io}T_\mathrm{oi}}{Y_\mathrm{o}}, \tag{3.15}$$

$$Z_{\text{in}-\infty} = Z_{\text{in}} - \frac{G_{\text{io}} G_{\text{ci}}}{G_{\text{co}}} \tag{3.16}$$

In the case of very low admittance Y_{S}, the current through the admittance would be negligible and the situation would be as in Fig. 3.3. Because the admittance is the inverse of impedance, this situation would mean that the output impedance of the source would be high. As it was discussed in the previous chapter, the output impedance of the PV module is high when the output voltage of the PV module is low. This means that the effect of the PV module on the converter dynamics is more severe in the CV region than in the CC region of the PV module.

The final closed-loop model of the converter can be solved by first calculating the open-loop transfer functions of the converter as in (3.7), then adding the effect of the PV module by using (3.14) and finally by solving the closed-loop transfer functions by (3.12).

4. CONVERTER DESIGN

In this chapter, two different boost-power-stage converters are designed. First one is named as Converter CM, because its design is based on the conventional design methods presented in [3] and [4]. The second converter is named as Converter NM, because its design is based on the charasteristics of the solar panel during the different climatic conditions including peaks in incident radiation. In [3], the designed converter is an interleaved boost, whereas in [4] it is a three-level boost converter. In this thesis, the design is based on a basic boost converter but comparison with the aforementioned publications is relevant since the basic principles in component sizing are the same.

4.1 Maximum Input Current and Voltage

Sizing factor (SF) is the ratio of solar inverter nominal power P_{nom} to the dc power of a PVG in STC $P_{\text{PVG-STC}}$ as in (4.1). Depending on the source, P_{nom} might be input [22] or output [14] power of the inverter. Input power is used in this thesis. Inverter might have one or two conversion stages, in which case both of the conversion stages must have the same power rating. So in the case of double-stage conversion, input power of a solar inverter is also the input power of a DC/DC converter. When $0 < SF < 1$, the inverter is undersized and for $SF > 1$, the inverter is oversized compared to the PVG. Optimal SF value has been studied widely, and there are various publications concerning it [22],[14],[23]. The main factors that affect the optimal value of SF are ambient temperature and irradiance patterns, incentives, protection method and efficiency of the inverter.

$$SF = \frac{P_{\text{nom}}}{P_{\text{PVG-STC}}} \tag{4.1}$$

Protection of a solar inverter can be implemented in several ways. One way is to shut down the inverter immediately when over-current is detected. Other way is to have a time delay before entering into protection mode and the power can be limited to acceptable level, e.g to nominal power. Protection can also be based on the temperature measurement of power semicoductors. The immediate shutdown decreases energy yield substantially if the inverter is undersized and incident radiation fluctuates heavily as in Fig. 2.3. On the other hand, if time delay and power limiting are used, it is possible to achieve greater energy yield by the same inverter. Power limiting can be done by moving the operation point away from the MPP by changing the input voltage to a higher level. [22]

The value of 0.7 for SF is used in this thesis since it is the widely used rule-of-thumb and thus represents the typical case. It is also assumed that the protection of the converter is implemented by limiting the output power to the level of nominal power. By using the sizing method presented in [3] and [4], the maximum input current of the converter for NAPS NP190Gkg PV module would be as follows:

$$I_{\mathrm{IN,MAX}} = \frac{P_{\mathrm{PVG\text{-}STC}} SF}{U_{\mathrm{MPP,MIN}}} \tag{4.2}$$

The maximum input current is 22.9 A when the values given in Chapter 2 and (4.2) are used. On the other hand, the maximum current that is possible to get from the NAPS NP190Gkg PV module in any climate condition is about 1.4 times the short-circuit current in STC, which equals to 11.2 A. This is the input current value used in the new design method. The difference between the current values of these two design methods is remarkable and it would be even greater if the higher value of SF would be used. For example by using unity SF, which is also a commonly used value, the maximum input current would be 32.8 A [22]. It is also essential to remember that by using the conventional design method, the output power of the converter is limited to be lower than the nominal output power of the PV module, whereas in the new design method the converter is designed to handle the maximum output power of the PV module.

In Chapter 2, the maximum OC output voltage of NAPS NP190Gkg PV module was found to be 36.5 V. Even if the output voltage mainly stays below this value when operating at the MPP, the converter should be able to handle the OC voltage as well. By adding some safety margin, the voltage rating of the components in both of the converters should be 50 V. Output voltage of the converter was selected to be 40V, because it is higher than the highest input voltage but still safe to handle. It should be noted that the input voltage of the inverter, which is connected to the grid, should have higher input voltage than the peak value of the grid voltage. However, the results presented in this thesis are also valid in the converters with higher voltage levels.

4.2 Inductor Design

First of all, the minimum value for the inductance to produce specified amount of current ripple is defined. Inductor voltage can be approximated by (4.3).

$$u_{\mathrm{L}} = L\frac{\mathrm{d}i_{\mathrm{L}}}{\mathrm{d}t} \approx L\frac{\Delta i_{\mathrm{L,pp}}}{\Delta t}, \tag{4.3}$$

where u_{L} is the inductor voltage, L is the inductance, i_{L} is the inductor current, $\Delta i_{\mathrm{L,pp}}$ is the inductor current peak-to-peak ripple value and Δt is the rising time of the inductor current, which is on-time of the switch. During the on-time, the inductor voltage equals to the input voltage in boost converter. The expression for inductor current ripple can

be solved by substituting (3.11) without parasitics into (4.3) yielding

$$\Delta i_{\mathrm{L,pp}} L = u_{\mathrm{L}} \Delta t = U_{\mathrm{in}} D T_{\mathrm{s}} = \frac{U_{\mathrm{in}}}{f_{\mathrm{s}}} - \frac{U_{\mathrm{in}}^2}{f_{\mathrm{s}} U_{\mathrm{o}}} \tag{4.4}$$

The inductor current ripple is at its highest value when the input voltage is half the output voltage, which can be found by calculating the partial derivative of (4.4) in respect to the input voltage. By substituting this information back to (4.4) and by solving the inductance, the minimum value of the inductance is found:

$$L = \frac{U_{\mathrm{o}}}{4 \Delta i_{\mathrm{L,pp}} f_{\mathrm{s}}} \tag{4.5}$$

Core material was selected to be Metglas, which is made of amorphous metal having high saturation flux density and low core losses. Maximum inductor current ripple was set to be 10% of the maximum input current. The maximum peak flux density was set to be 90% of the saturation flux density of the core. These selections were made to be consistent with [3] and [4]. Values that were used as a specification for the inductor design are presented in Table 4.1.

Table 4.1: Inductor Design Specification

Symbol	Description	Value	Unit
J	Current density	500	A/cm^2
K	Window utilization factor	0.4	
B_{MAX}	Maximum peak flux density	1.4	T

Core selection was based on the core area product $WaAc$, which is defined in (4.6). The complete derivation of this equation is presented in [24]

$$W_{\mathrm{a}} A_{\mathrm{c}} = \frac{L I_{\mathrm{L,p}}^2 10^4}{B_{\mathrm{max}} J K}, \tag{4.6}$$

where $I_{\mathrm{L,p}}$ is the peak value of the inductor current. With 10% ripple, the inductor current peak value is 1.05 times maximum input current. L is the minimum inductance value according to (4.5). The result of (4.6) is in cm^4, which is the same unit as in Metglass datasheets. Few metglass microlite toroidial cores with distributed airgap were selected as core candidates. Cores of Metglass C-series that were used in [3] and [4] are too large to be used in this application.

After core selection, the preliminary number of turns was calculated by using (4.7). It is called preliminary, because the permeability of the core decreases when the magnetic flux in the core increases, which is dependent on the DC current through the winding and on the number of turns. This means that selecting the number of turns is an iterative process. Nominal relative permeability of 245 given in the datasheet [25]

was selected to be the preliminary relative core permeability. [4]

$$N_{\mathrm{i}} = \sqrt{\frac{L l_{\mathrm{m}}}{\mu_0 \mu_{\mathrm{e}} A_{\mathrm{e}}}}, \tag{4.7}$$

where l_{m} is the core magnetic path length, μ_0 is the permeability of free space, μ_{e} is the relative core permeability and A_{e} is the cross-sectional area of the core. The preliminary number of turns was substituted in (4.8), which gives the magnetic field strength in Oersteds (Oe).

$$H = \frac{0.4 N I_{\mathrm{dc}}}{l_{\mathrm{m}}}, \tag{4.8}$$

where N is the number of turns and I_{dc} is the dc bias current through the coil. In this case, it equals to $I_{\mathrm{IN,MAX}}$

By using the graph that is presented in the Mircolite datasheet, where core permeability is presented as a function of magnetic field strength, new and more accurate value for the core permeability was found. Aforementioned steps should be repeated as many times as it is required to find the value of the core permeability. In practice, this means that last two iteration rounds must lead to the same number of turns. In this case three iteration rounds was sufficient. Also higher temperature decreases the inductance of the inductor but this was not taken into account in the calculations. [25]

Required cross-sectional area A_{w} of the wire was calculated directly from the current density J specification given in Table 4.1 as

$$A_{\mathrm{w}} = \frac{I_{\mathrm{L,p}}}{J} \tag{4.9}$$

Calculated cross-sectional area was then rounded to the closest standard value. Now the dc resistance R_{DC} of the wire can be calculated as

$$R_{\mathrm{DC}} = \rho \frac{l_{\mathrm{w}}}{A_{\mathrm{w}}}, \tag{4.10}$$

where ρ is the conductivity of wire material, l_{w} is the length of the wire. Six inductors was designed based on Equations (4.1) - (4.10) and the results are presented in Table 4.2. First three rows are calculated by using the conventional design method and three latter rows are calculated by using the new design method.

As it is visible from the Table 4.2, the conventional design method leads to lower inductance value and to higher wire gauge than the new design method. On the other hand, DC resistance of the inductors that are designed by using the conventional method are lower, due to the less number of turns with larger wire gauge. This leads to lower power losses as presented later. MP3310LDGC and MP2510LDGC were selected,

Table 4.2: Results of the inductor design

Core	V_{core} (cm^3)	$I_{\text{IN,MAX}}$ (A)	L (μH)	N	R_{dc} (mΩ)	A_{w} (mm^2)
MP3210LDGC	3.52	22.9	43	20	6	4
MP3310LDGC	5.34	22.9	43	13	4	4
MP3505MDGC	5.34	22.9	43	13	4	4
MP2610LDGC	2.48	11.2	89	25	11	2.5
MP2510LDGC	1.89	11.2	89	32	14	2.5
MP2310MDGC	2.38	11.2	89	25	11	2.5

because they were the only cores in Table 4.2 available from the manufacturer.

Power losses of the inductor are distributed within the core and winding. Thus, the total power loss consists of core and copper losses. Core losses are the sum of hysteresis, eddy current and residual losses [26]. Copper losses can be further divided into the losses caused by the direct current flowing through the resistance of the winding and into the losses caused by the alternating current due to skin and proximity effects. At high frequencies, the current density is higher in the outer layer of the conductor. This phenomenon is called skin effect. Alternating current flowing through a conductor causes traverse field into other conductor that is located next to it. This phenomenon is called proximity effect. The losses caused by alternating current was calculated by using the methods presented in [4], but since its share of the total power loss was only about 0.5%, it was omitted from the loss calculation. The equations needed to calculate the total power loss of the inductor are presented next. The peak value of the AC flux $B_{\text{AC,PEAK}}$ can be calculated as given in (4.11) [4].

$$B_{\text{AC,PEAK}} = \frac{\mu_0 \mu_{\text{real}} \Delta i_{\text{L,pp}} N}{2 l_{\text{m}}}, \tag{4.11}$$

where μ_{real} and N are final values from the iterative inductor design and the rest are predefined quantities. The result is substituted to (4.12) in order to find the value for inductor core loss P_{CORE}.

$$P_{\text{CORE}} = m \left(275 B_{\text{AC,PEAK}}^{2.6} f_{\text{s}} + 0.114 B_{\text{AC,PEAK}}^{2} f_{\text{s}} \right), \tag{4.12}$$

where m is the mass of the core. Eq. (4.12) is given in the Microlite datasheet [25] including all of the aforementioned core loss components. The DC part of the copper losses can be simply calculated by (4.13).

$$P_{\text{CU,DC}} = I_{\text{DC}}^2 R_{\text{DC}}, \tag{4.13}$$

where I_{DC} is the direct current flowing through the winding, which is the input current in the case of a boost-power-stage converter.

By summing the core and copper losses and by neglecting the copper losses caused by alternating current, the total power loss is as given in (4.14).

$$P_{\mathrm{TOT}} = P_{\mathrm{CORE}} + P_{\mathrm{CU,DC}} \tag{4.14}$$

The power loss calculation was made for both of the selected inductors in STC. The results are presented in Table 4.3. As it is shown, the conventional design method leads to a larger core, and thus also higher core loss than the new design method. On the other hand, the copper loss is lower due to the less number of turns with larger wire gauge. By using these values and cores, it seems that total power losses in STC are higher when the new design method is used.

Table 4.3: Results of power loss calculation in STC

Core	P_{CORE} (W)	$P_{\mathrm{CU,DC}}$ (W)	P_{TOT} (W)
MP3310LDGC	0.50	0.27	0.77
MP2510LDGC	0.26	0.88	1.14

According to Table 4.3, if the cost is the most important factor, then the new design method should be used. But if the efficiency is the most important factor, then the conventional design method might be better option.

The inductors were built based on the design results presented in Table 4.2 by using the selected cores MP3310LDGC and MP2510LDGC. The winding of the 43-μH inductor was divided into two parellel wires with the wire diameter of 1.6mm, because the wire thicker than 1.8mm was not available from the distributor. It was also easier to wind two thin wires instead of one thick wire. The inductance value of both of the inductors was measured to verify the design. The value of the inductance was measured by the means of the frequency response analyser Model 3120 of Venable Instruments with an impedance measurement kit.

The measurement setup is presented in Appendix A. 12V/120Ah lead acid battery was used to produce high enough bias current through the inductor winding and Chroma DC electric load was used to keep the bias current constant. The impedance was measured with four different bias current values. The value of the inductance was found by fitting the impedance graph of the RL circuit model to the measured impedance graph.

The inductance measurements revealed that the inductance value dropped steeply as a function of bias current, steeper than it was predicted in the datasheet. Two similarly designed inductors were connected in series to get enough inductance and this solution was also used in the converter prototypes. The measured and fitted impedance curves of the series connected inductors are presented in Appendix A and the resulting values of the inductances are presented in Table 4.4 and Table 4.5, respectively.

Table 4.4: Measurement from 89-μH inductor

Measurement current (A)	Resistance (mΩ)	Inductance (μH)
2.6	19.7	173
7.33	19.7	120
7.89	19.7	110
11	19.7	68

Table 4.5: Measurement from 43-μH inductor

Measurement current (A)	Resistance (Ω)	Inductance (μH)
2.6	6.4	85
7.33	6.4	72
7.89	6.4	69
23	6.4	38.2

As it is shown in Table 4.4, the inductance value of the 89-μH inductor is still not as large as it was designed to be when the DC current is 11A. On the other hand, when the DC current is 2.6A, inductance is much larger than expected. The inductor core with an air gap might give less variation on inductance. That might be one of the reasons, why such cores are commonly used in power converters. Such an alternative for the core would have been Microlite 100u serie of Metglass.

The current values of 2.6A, 7.33A and 7.89A in Table 4.4 corresponds the operating points, which are used in the frequency response measurements presented in Chapter 5. The measured inductance values are substituted to the model to fit the predicted frequency responses to the measurements. As the inductance is larger than the desired value of 89-μH at the operating points that are used in the measurements, the inductor is adequate for the purposes of this thesis. Similar observations can be made on the 43-μH inductor based on Table 4.5 as for the 89-μH inductor.

4.3 Selection of MOSFET and Diode

In this thesis, the selection of the power semiconductors for the converter prototypes was made as follows: First, a group of component cadidates was selected by their voltage and current ratings, case type and availability. Then the component with the lowest total power loss was selected from the group. As it was mentioned in the previous chapter, the minimum voltage rating for the components in both of the converters was specified to be 50 volts. The power switch was selected to be MOSFET, since it is the best option for the used switching frequency and power range. The Schottky diode was selected, because it has low forward voltage drop and negligible reverse recovery loss even though it has larger reverse leakage current than the silicon pn-junction diode [27].

The typical waveforms of the driver output voltage u_{dri}, inductor current i_{L}, MOSFET current i_{sw} and diode current i_{d} are presented in Fig. 4.1. Inductor current flows through the switch when it is on and through the diode when the switch is off.

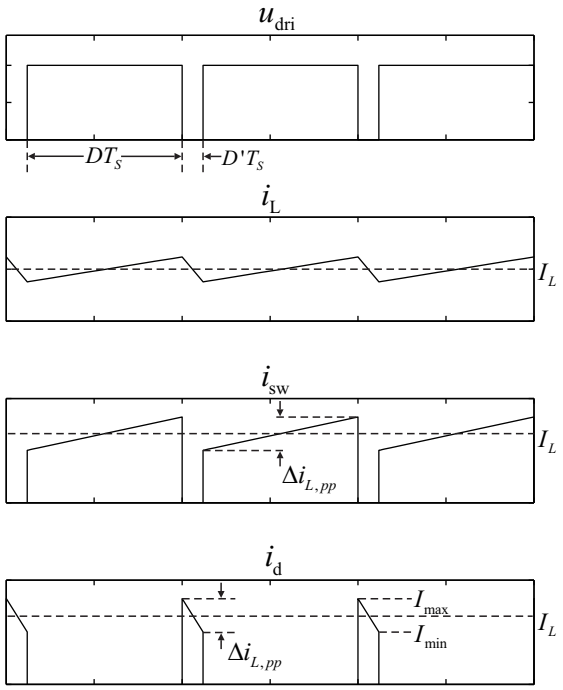


Figure 4.1: Current waveforms in semiconductors.

The root mean square (RMS) value of the switch current $I_{\mathrm{sw,rms}}$ can be calculated as given in (4.15) based on the current waveform presented in Fig. 4.1 [19]. The replacement of the duty ratio D in (4.15) by the complement of the duty ratio D' yields to the RMS value of the diode current $I_{\mathrm{d,rms}}$ as presented in (4.16).

$$I_{\mathrm{sw,rms}} = I_{\mathrm{L}}\sqrt{D}\sqrt{1+\frac{1}{3}\left(\frac{\Delta i_{\mathrm{L,pp}}}{2I_{\mathrm{L}}}\right)^2}, \tag{4.15}$$

$$I_{\mathrm{d,rms}} = I_{\mathrm{L}}\sqrt{D'}\sqrt{1+\frac{1}{3}\left(\frac{\Delta i_{\mathrm{L,pp}}}{2I_{\mathrm{L}}}\right)^2}, \tag{4.16}$$

where I_{L} is the average value of the inductor current, which equals to the input current of the boost-power-stage converter. D' is the complementary duty ratio. The peak-to-

peak ripple of the inductor current $\Delta i_{\mathrm{L,pp}}$ can be solved from (4.4) yielding

$$\Delta i_{\mathrm{L,pp}} = \frac{U_{\mathrm{in}} D T_{\mathrm{s}}}{L}, \tag{4.17}$$

where D is the duty cycle at the operation point where the RMS value of the current is determined. The power loss of the semiconductor is quadratically dependent on the RMS value of the current, which means that higher current produces higher loss. It was stated in [3] that both of the semiconductors produce the highest loss when the input voltage of the converter is in its minimum value. Small value of input voltage means that the duty cycle has a large value and the complementary duty cycle D' is has a small value. The current waveforms in Fig. 4.1 corresponds to this situation. According to (4.15), the RMS value of the current is heavily affected by the duty cycle and average inductor current but the effect of inductor current ripple is not that significant. If the average inductor current, i.e. the input current of the converter, is constant, the RMS value of the current is mainly determined by the duty cycle. This is a realistic assumption when operating in the CC region of the PV module. In the case of a large value of D and a small value of D', the power loss of the switch is higher than the power loss of the diode. Respectively, if D has a small value and D' has a large value, the power loss of the diode is higher than the power loss of the switch.

The power loss of the diode increases when the duty ratio decreases, which means that the input voltage of the converter, i.e. the output voltage of the PV module increases. This is valid in the CC region and in the MPP but not anymore in CV region, since the output current of the PV module starts to decrease. This means that the power loss of the diode increases up to the MPP and starts to decrease if the voltage is still increased. The diode power loss was calculated at different operation points of the curve in Fig. 2.10 and it was verified that the maximum power loss of the diode occurs at the MPP.

As a summary, the MOSFET power loss should be calculated at the minimum input voltage and the power loss of the diode should be calculated at the MPP. The power losses of Converter NM was calculated this way. The power losses of Converter CM were calculated in the minimum input voltage for both of the semiconductors. The calculated RMS current values of both of the design methods are presented in Table 4.6.

Table 4.6: Calculated RMS currents of the switch and diode

$I_{\mathrm{IN,MAX}}$ (A)	$I_{\mathrm{sw,rms}}$ (A)	$I_{\mathrm{d,rms}}$ (A)
22.9	21.3	8.7
11.2	10.4	8.7

The current values obtained according to the conventional design method are presented in the first row of Table 4.6. The current values obtained according to the new design method are presented in the second row, respectively. As it can be seen, there

is a significant difference in the RMS current of the switch between the two design methods. Surprisingly, the diode RMS current became the same in both of the design methods. Reason for this is that the higher input current is used in the conventional design method but the diode current is calculated at the same operation point as the current of the switch.

Now when the RMS values of the currents through the semiconductors are known, the power losses can be approximated. The power loss calculations of the switch are based on [28] and the detailed derivation of (4.18)-(4.26) can be found from there. The total power loss $P_{\mathrm{sw,tot}}$ of MOSFET switch is the sum of conduction losses $P_{\mathrm{sw,sw}}$ and switching losses $P_{\mathrm{sw,c}}$ [28].

$$P_{\mathrm{sw,tot}} = P_{\mathrm{sw,c}} + P_{\mathrm{sw,sw}} \tag{4.18}$$

MOSFET power switch conducts during the on-time. It can be modelled as a resistor $R_{\mathrm{ds,on}}$. Resistance of $R_{\mathrm{ds,on}}$ is given in the datasheet being dependent on the drain-souce voltage and junction temperature. When the resistance and current is known, the power loss during on-time can be estimated as follows

$$P_{\mathrm{sw,c}} = R_{\mathrm{ds,on}} I^2_{\mathrm{sw,rms}}, \tag{4.19}$$

In reality, the power switch turns on and off in finite time, introducing power losses. The switch-on process of MOSFET can be divided into two parts: During the first part, the drain-source voltage is the same as during the off-time and the drain current is rising. This time period is called the current rise time t_{ri} given in the datasheet. During the second part, the current is in the level defined by the other circuit elements and the drain-source voltage is falling. This time period is called voltage fall time t_{fu} and it can be calculated as presented in (4.20)-(4.22). The voltage fall time is further divided into two parts t_{fu1} and t_{fu2} since the drain-source voltage is approximated to have two linear slopes. The idea is to take into account the non-linear behavior of the drain-source voltage by simpification [28].

$$t_{\mathrm{fu}} = \frac{t_{\mathrm{fu1}} + t_{\mathrm{fu2}}}{2} \tag{4.20}$$

$$t_{\mathrm{fu1}} = (U_{\mathrm{o}} - R_{\mathrm{ds}} I_{\mathrm{d,on}})\, R_{\mathrm{g}} \frac{C_{\mathrm{gd1}}}{U_{\mathrm{dr}} - U_{\mathrm{plateau}}}, \tag{4.21}$$

where U_{o} is the output voltage of the converter, R_{g} is the gate resistor, C_{gd1} is the capacitance value of C_{rss} read from the datasheet when $U_{\mathrm{ds}} = U_{\mathrm{o}}$, U_{dr} is the output voltage of the driver circuit and U_{plateau} is the plateau voltage, which is also given in

the datasheet [28]. The second part of the voltage can be given as follows

$$t_{\mathrm{fu2}} = (U_{\mathrm{o}} - R_{\mathrm{ds}} I_{\mathrm{d,on}})\, R_{\mathrm{g}} \frac{C_{\mathrm{gd2}}}{U_{\mathrm{dr}} - U_{\mathrm{plateau}}} \tag{4.22}$$

where C_{gd2} is the capacitance value of C_{rss} given in the datasheet when $U_{\mathrm{ds}} = U_{\mathrm{o}}/2$. The switch-off process of MOSFET corresponds to the switch-on process in the reverse order and so the time period t_{ru} during which the drain current is constant and drain-source voltage is rising can be calculated as in (4.23)-(4.25). The other part of the switch-off period is called current fall time t_{fi} also given in the datasheet [28].

$$t_{\mathrm{ru}} = \frac{t_{\mathrm{ru1}} + t_{\mathrm{ru2}}}{2}, \tag{4.23}$$

$$t_{\mathrm{ru1}} = (U_{\mathrm{o}} - R_{\mathrm{ds}} I_{\mathrm{d,on}})\, R_{\mathrm{g}} \frac{C_{\mathrm{gd1}}}{U_{\mathrm{plateau}}} \tag{4.24}$$

$$t_{\mathrm{ru2}} = (U_{\mathrm{o}} - R_{\mathrm{ds}} I_{\mathrm{d,on}})\, R_{\mathrm{g}} \frac{C_{\mathrm{gd2}}}{U_{\mathrm{plateau}}} \tag{4.25}$$

The switching losses can be calculated according to the defined switch-on and switch-off events as given in (4.26).

$$P_{\mathrm{sw,sw}} = U_{\mathrm{o}} I_{\mathrm{drain,on}} \frac{t_{\mathrm{ri}} + t_{\mathrm{fu}}}{2} f_{\mathrm{s}} + U_{\mathrm{o}} I_{\mathrm{drain,off}} \frac{t_{\mathrm{ru}} + t_{\mathrm{fi}}}{2} f_{\mathrm{s}}, \tag{4.26}$$

where $I_{\mathrm{drain,on}}$ is the drain current in the beginning of t_{fu} time period and $I_{\mathrm{drain,off}}$ is the drain curren in the beginning of t_{fi} time period [28].

The following criteria was used to select a group of power switch candidates: Maximum voltage rating at least 50V, maximum current ratings as given in Table 4.6, a case that is easy attach to a heat sink and the switch should also be available from the component distributors. The power loss calculations of the MOSFET candidates for the converter designed by using the new design method are presented in Table 4.7. The worst-case junction temperature was selected to be 100°C as proposed in [27].

As it is shown in Table 4.7, IPA057N06N3 has lowest total power loss and thus it was selected to the converter which was designed by using the new design method. Similar comparison was also made for the converter that was designed by using the conventional design method leading to the same MOSFET as with the new design method. Thus, IPA057N06N3 was used in both of the converters with calculated total power loss of 4.7 W by using the conventional design method and 2.6 W by using the new design method. These values were used in the thermal design. Note that if more

Table 4.7: Results of MOSFET power loss calculation

Component	$P_{\mathrm{sw,c}}$ (W)	$P_{\mathrm{sw,sw}}$ (W)	$P_{\mathrm{sw,tot}}$ (W)
STD30NF06	2.9	3.6	6.5
SI7478DP	0.9	4.0	4.9
FDP42AN15A0	6.7	1.2	7.9
IPD400N06N	5.2	1.5	6.7
IPA057N06N3	0.7	1.9	2.6
STP16NF06L	11.8	1.5	13.3
IPD250N06N3	3.0	0.2	3.2

detailed component optimization would be used, the result might be quite different than in this case. For example, the cost of the component might be included to the optimization and a greater group of component candidates could have been evaluated.

Schottky diodes turns on and off faster than $p-n$ junction diodes and have negligible reverse recovery loss [27]. For this reason, the total power loss of the diode $P_{\mathrm{d,tot}}$ was calculated by taking account only the conduction loss $P_{\mathrm{d,cond}}$ and the power loss caused by reverse leakage current during the diode off time $P_{\mathrm{d,rev}}$ as follows

$$P_{\mathrm{d,tot}} = P_{\mathrm{d,cond}} + P_{\mathrm{d,rev}} \tag{4.27}$$

The conduction loss of the diode can be calculated as defined in (4.28), which has also been used in [3].

$$P_{\mathrm{d,c}} = I_{\mathrm{d,rms}} U_{\mathrm{d}}, \tag{4.28}$$

where $I_{\mathrm{d,rms}}$ is the RMS current of the diode given in Table 4.6 and U_{d} is the forward voltage drop of the diode given in the datasheet. Reverse current loss $P_{\mathrm{d,rev}}$ can be calculated as presented in (4.29) [29].

$$P_{\mathrm{d,rev}} = U_{\mathrm{d,rev}} I_{\mathrm{d,rev}} D, \tag{4.29}$$

where $U_{\mathrm{d,rev}}$ is the reverse voltage, which in this case equals to output voltage of the converter U_{o}, $I_{\mathrm{d,rev}}$ is the reverse leakage current of the diode given in the datasheet and D is the duty cycle of the MOSFET. Multiplication with D is needed, because the reverse current loss occurs only during the off time, which occurs during the on time of the switch. If the conventional design method would be used, the input voltage would be 5.8 V meaning that the duty cycle is 0.86. If the new design method would be used, input voltage would be 28.5 V, because that is the MPP voltage of the $I-U$ curve of Fig. 2.10 meaning that the duty cycle is 0.29. The reverse current of the selected diode is so small that it will lead to the same total power loss despite of the duty cycle used and this is why the same diode and heat sink was used in both of the converters.

The same criteria was used to select a group of diode candidates as with the power switch. The power loss calculations of the diode candidates are presented in Table 4.8 by using the duty cycle of 0.86 and the junction temperature of 100°C.

Table 4.8: Results of the diode power loss calculation

Component	$P_{\mathrm{d,cond}}$ (W)	$P_{\mathrm{d,rev}}$ (W)	$P_{\mathrm{d,tot}}$ (W)
10WT10FN	5.729	0.003	5.7
SS10P6	4.601	0.017	4.6
30PT100	4.340	0.021	4.4
DSSK 40-008B	3.559	1.060	4.6
STPS20L60CT	4.688	0.274	5.0
STPS10L60D	4.774	0.274	5.0
STPS20M60S	3.472	0.068	3.5

As it is shown in Table 4.8, STPS20M60S has the smallest total power loss and thus it was selected to be used in both of the converters. Result was verified by calculating the conduction loss of the selected component according to following equation provided in the STPS20M60S datasheet

$$P_{\mathrm{d,c}} = 0.380 I_{\mathrm{d,avg}} + 0.0063 I_{\mathrm{d,rms}}^2, \tag{4.30}$$

where $I_{\mathrm{d,avg}}$ is the average value of the diode current. (4.30) is a commonly used equation where 0.380 is the treshold voltage of the diode and 0.0063 is the dynamic resistance of the diode. Average value of the diode current can be calculated as shown in (4.31) by using the notation of Fig. 4.1 [30, 231].

$$I_{\mathrm{d,avg}} = \frac{D' \left(I_{\mathrm{max}} + I_{\mathrm{min}} \right)}{2}, \tag{4.31}$$

where I_{max} is the maximum value of the inductor current and I_{min} is the minimum value of the inductor current. The conduction loss of the diode was calculated by using the conventional design method, where the input current was 22.9 A and the input voltage was 5.8 V. The conduction loss was calculated also by using the new design method where the input current was 11.2 A and the input voltage was the MPP value of 28.5 V. The results of the calculations are presented in Table 4.9.

Table 4.9: Calculated conduction loss of STPS20M60S diode

$I_{\mathrm{IN,MAX}}$ (A)	$I_{\mathrm{d,avg}}$ (A)	$P_{\mathrm{d,c}}$ (W)
22.9	3.3	1.7
11.2	7.3	3.2

As it can be seen from the calculated values in Table 4.9, the diode conduction loss in the lower row obtained by the new method is quite close to the value presented in Table

4.8. It is not mentioned in the datasheet at which junction temperature the constant values in (4.31) are given. Those values are probably given at higher temperature than at 100°C, which gives a good explanation to the difference. The power loss was also calculated at the temperatures 110°C and 125°C by using (4.28). The results were 3.4 W and 3.3 W respectively, which is close to the 3.2 W in Table 4.9.

The result that was obtained by using the conventional design method is interesting, since it predicts 50% smaller power loss if (4.30) is used insted of (4.28). The reason for the small power loss is the small average value of the current which further is caused by using a large value of D and a small value of D' in the conventional design method. Conclusion is that using (4.30) with the conventional design method will lead to the underestimation of the diode conduction loss and thus (4.28) should rather be used. The power loss of 3.5 W was used as a baseline value for the heat sink sizing of the diode.

4.4 Thermal Design

Heat transfer from a semiconductor to ambient air through a heat sink can be described by thermal equivalent circuit, which is analogous to an electric circuit. The temperature difference is equivalent to the voltage difference, the dissipated power is equivalent to the electric current and the thermal resistance is equivalent to the electrical resistance. The goal is to find a proper value for the thermal resistance of the heat sink which gurantees that the $p-n$ junction temperature of the semiconductor will not be excessively high. The thermal equivalent circuit including the power loss of the semiconductor P_{tot} and the thermal resistances from the $p-n$ junction of the semiconductor to the ambient air is presented in Fig. 4.2. The thermal equivalent circuits of the diode and MOSFET are the same in this thesis, but of course the numerical values are different. [27]

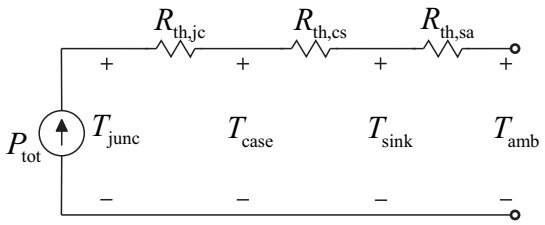


Figure 4.2: Thermal equivalent circuit [27].

In Fig. 4.2, $R_{\text{th,jc}}$ is the thermal resistance between the $p-n$ junction and the semiconductor case, $R_{\text{th,cs}}$ is the thermal resistance between the case and the heat sink, $R_{\text{th,sa}}$ is the thermal resistance between the heat sink and the ambient temperature T_{amb}, T_{junc} is the $p-n$ junction temperature and T_{case} is the temperature of the semiconductor case.

The diode and MOSFET are both directly attached to their heat sinks with only thermal grease in between. In this case, the value of $R_{\text{th,cs}}$ is very small and thus it is

approximated to be zero. $R_{\text{th,jc}}$ is given in the semiconductor manufacturer datasheet, T_{junc} is selected to be 110°C for the diode and 100°C for the MOSFET, T_{amb} is specified to be 50°C. P_{tot} of the diode and MOSFET were calculated in the previous chapter. Only unknown value $R_{\text{th,sa}}$ can be solved from the circuit of Fig. 4.2 yielding

$$R_{\text{th,sa}} = \frac{T_{\text{junc}} - T_{\text{amb}} - P_{\text{tot}} R_{\text{th,jc}}}{P_{\text{tot}}}. \tag{4.32}$$

Maximum allowable value of the thermal resistance $R_{\text{th,sa}}$ was calculated by using (4.32). The calculated thermal resistances and the values used in the calculations are presented in Table 4.10.

Table 4.10: Results of the thermal design

	Method 1 IPA057N06N3	Method 2 IPA057N06N3	Both converters STPS20M60S
T_{amb} (°C)	50	50	50
T_{junc} (°C)	100	100	110
P_{tot} (W)	4.7	2.6	3.4
$R_{\text{th,jc}}$ (°C/W)	4	4	1
$R_{\text{th,sa}}$ (°C/W)	6.6	15.2	16.6
Selected heat sink	530402B00150G	534202B03453G	581102B02500G
$R_{\text{th,sa,sel}}$ (°C/W)	6.5	14.7	15.4

The heat sinks were selected from the Aavid Thermalloy heat sink catalog and the number series in the 6th row are part numbers. $R_{\text{th,sa,sel}}$ in the last row is the thermal resistance of the selected heat sink given in the catalog. As it is shown in Table 4.10, the heat sinks were selected to have lower thermal resistance than the maximum allowable values. This way it is guranteed that the temperature of the $p-n$ junction stays below the specified limit. The diode was allowed to have higher temperature than MOSFET, because this particular heat sink was designed to be used.

4.5 Control Design and Selection of Input Capacitor

The specification of the control design and the selection of the input capacitor for both of the converters is to have at least 15dB attenuation from the output voltage to the input voltage at the frequency of 100Hz, low input voltage ripple and stable design. It was also required that the input capacitor should be ceramic, because it has longer lifetime expectancy than an electrolytic capacitor. The control design of the converter implemented by using the new design method is presented next. The principles of the control design is similar for both of the converters.

As it is shown in Fig. 5.8, the low-frequency phase of the control-to-input voltage transfer function starts from 180 degrees, which means that the conventional way of subtracting the measured input voltage from the reference voltage would lead to instability. This problem can be solved by interchanging the signs of input voltage reference

and feedback signal, which means that the phase and gain margins have to be read from the zero degree level of the bode plot instead of -180 degrees.

The control design was carried out by assuming that the component values would be constant despite the changes in the operating point, because usually the detailed values of the parasitic resistances etc. are not known in this stage. More accurate bode plots are provided in Chapter 5, where it is taken into account that the inductance and capacitance values are heavily affected by the operating point.

The loop gain of the input voltage control loop L_{in} is presented in Fig. 4.3, when the gain of the integral controller is unity and the capacitance of the input capacitor is 10μF. The dotted line represents the maximum input voltage condition and the solid line represents the minimum input voltage condition. As it can be seen, peaking in the CC region causes difficulties in control design. It is also visible that the control design should be carried out by using the minimum input voltage because of highest gain. On the other hand, closed-loop reverse voltage transfer ratio $T_{\text{oi-c}}$ has highest value when the input voltage is highest. This means that both the minimum and maximum input voltage conditions should be considered in control design. The reason for the high peaking is the high output impedance of the PV module in the CC region, low ESR value of the input capacitor and low DC resistance value of the inductor.

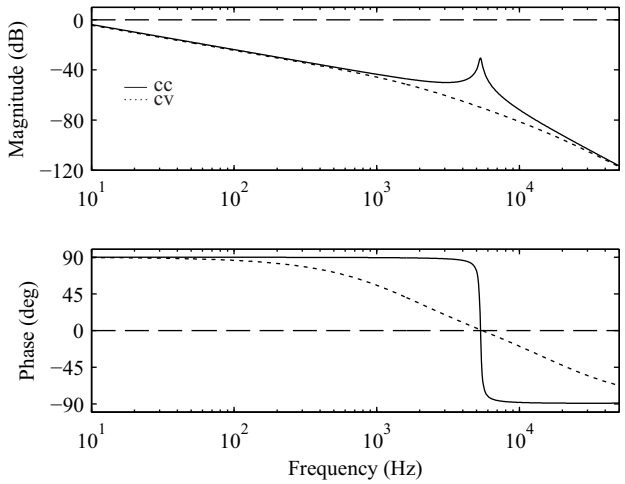


Figure 4.3: Loop gain of the input voltage control loop L_{in}.

The damping circuit consisting of series connected resistor and capacitor was added in parallel with the input capacitor. The capacitance value of the damping circuit was selected to equal the input capacitance and resistance value was selected to equal the characteristic impedance Z_{o} of the converter resonant circuit, which can be calculated by using (4.33) [31].

$$Z_{\text{o}} = \sqrt{\frac{L}{C_1}} \tag{4.33}$$

The damping network was added to the model by using the information that the

soure admittance Y_S equals to the sum of PV module output admittance and damping network admittance. L_{in} and $T_{oi\text{-}c}$ was plotted with different input capacitor values and the optimal value was found to be 10μF.

The loop gain of the input voltage control loop L_{in} is presented in Fig. 4.4, after the addition of the damping circuit. The dotted line represents the maximum input voltage condition and the solid line represents the minimum input voltage condition. Also the gain of 35dB of the integral controller is included leading to the phase margin of 83 degrees and the gain margin of 16 decibels predicting stable design.

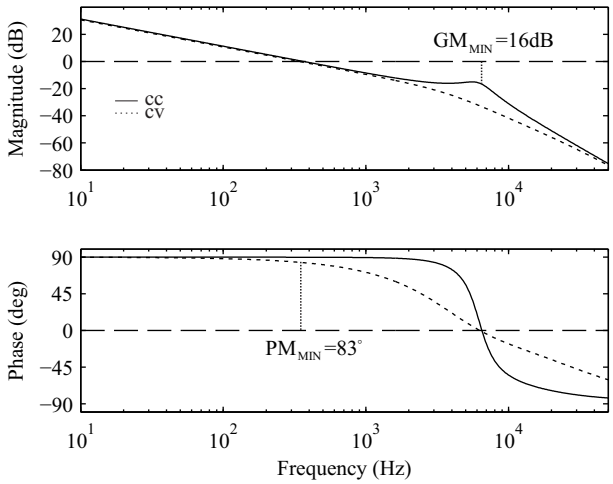


Figure 4.4: Loop gain of the input voltage control loop L_{in} when the damping circuit is added.

The closed-loop reverse voltage transfer ratio $T_{oi\text{-}c}$ is presented in Fig. 4.5 after addition of the damping circuit and the gain of 35dB of the integral controller. The dotted line represents the maximum input voltage condition and the solid line represents the minimum input voltage condition. As it is visible, the attenuation from the output voltage to the input voltage is 13dB at the frequency of 100Hz when the input voltage is 5 volts, and 25dB when the input voltage is 31 volts. Thus, the attenuation is varying between these limits being close to the specification.

The reduction of the PV module power output due to the input voltage ripple of the converter can be calculated by means of (4.34), which has been derived in [10] based on (2.1).

$$P_r = U_{r,rms}^2 \frac{I_{MPP}}{U_{MPP}} \left(1 + \frac{U_{MPP}}{2N_s akT/q}\right), \tag{4.34}$$

where $U_{r,rms}$ is the rms value of the ripple voltage, I_{MPP} is the output current of the PV module at the MPP and U_{MPP} is the output voltage of the PV module at the MPP. The reduction at NAPS NP190GKg PV module power output was calculated at the MPP in the STC by using the rms value of the switching frequency ripple voltage component obtained by simulation and measurement. The result was 20 mW, which

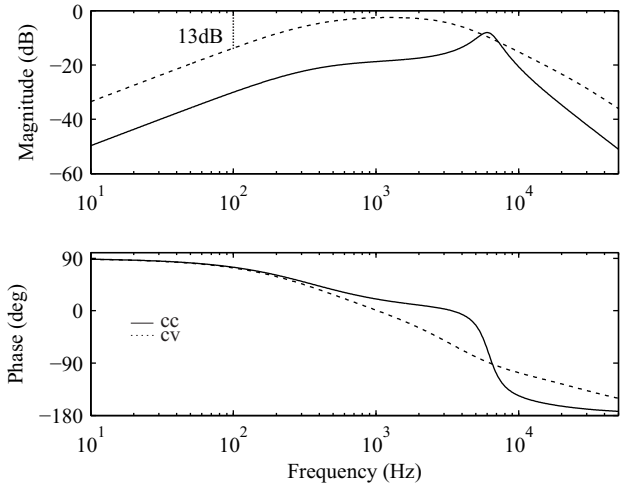


Figure 4.5: Closed-loop reverse voltage transfer ratio $T_{\text{oi-c}}$

means that the effect of high-frequency ripple on the energy yield is negligible and that the capacitance of the input capacitor is sufficient from this viewpoint.

All that can be said about the effect of double-line-frequency ripple on the PV module power loss is that it depends on the capacitance of the dc-link capacitor and that the capacitance can be somewhat smaller because of the low value of $T_{\text{oi-c}}$ at the double-line-frequency. During the measurements of the prototype converters, the output voltage was constant, so the only variation in the input voltage was caused by the switching frequency ripple voltage.

If it would be most desirable to have as low $T_{\text{oi-c}}$ at the double-line-frequency as possible, it can be done by increasing the damping capacitor and by increasing the resonant frequency, which can be done by decreasing the inductance of L or capacitance of C_1. This would cause the switching frequency component of the input voltage to increase as a drawback. The benefits would be smaller capacitance requirement for the dc-link and input capacitors as well as smaller inductance requirement. This is an interesting option if the increased high-frequency component of the input voltage ripple is not an issue.

The controlling of the converter designed by using the conventional design method was carried out by using the same conctroller as with the other converter. The damping resistor was selected to be half of the presented value, the input and damping capacitor capacitor was selected to be twice the presented value. By using these values, the electrical parameters of the two converters are similar and the comparison between the two design methods is relevant.

The most interesting differences between the designed converters are presented in Table 4.11. As it is shown, the volume of the core is significantly smaller when the new design method is used. On the other hand, the mass of the inductor copper is bigger because of smaller wire gauge and higher number of turns. The mass of the copper was calculated based on the mean turns lenght, the number of turns and the density of copper.

If MP3210LDGC core would be used instead of the selected MP3310LDGC, the volume of the core would be 3.52cm^2 as presented in Table 4.2. In this case, the number of turns should be 20 leading to 41 grams as a mass of the inductor copper. Thus, the percentage decrease of the core volume would be 46%, and the percentage decrease of the inductor copper mass 25%. Thus, it cannot be denied that the new design method leads to cost savings. Unfortunately this core was not available from the manufacturer, so MP3310LDGC had to be used in the prototype converter.

Table 4.11: Summary of the main differences between the converter prototypes.

	CM	NM	Decrease in %
Volume of the core (cm^2)	5.34	1.89	65
Mass of the inductor copper (g)	29	31	-8.4
Thermal resistance of the heat sink (K/W)	6.5	14.7	-126
Capacitance of input capacitor (μF)	20	10	50
Capacitance of damping capacitor (μF)	20	10	50
Width of the PCB copper (mm)	9.6	4.8	50
Current rating of the connectors (A)	23	12	47.8

As it is shown in Table 4.11, the heat sink of the MOSFET have to be much bigger when the conventional design method is used. Also capacitance requirement is higher as discussed earlier. The width requirement of the PCB copper was calculated by specifying that the tolerable increase in temperature is to be 30 degrees and that the copper thickness is 35μm. Also the connectors were selected to the converters according the values presented in Table 4.11.

5. MEASUREMENTS

All measurements presented in this chapter has been made by using agilent E4360A solar array simulator (SAS) as a source and three series connected 12V batteries in parallel with Chroma 63103A current sink as a load. The same SAS is proved to emulate the dynamical properties of NAPS NP190GKg PV module accurately enough in the prior research [9]. The values of NAPS NP190GKg PV module in STC presented in Table 2.1 was used in the SAS. The measurements were made in the CC region, at the MPP and in the CV region with the voltage and current values of 5V/7.98A, 25.9V/7.33A and 31V/2.6A, respectively.

5.1 Prototypes

Both prototypes of the designed converters are divided into two circuit boards. The first circuit board includes the power-stage, the driver circuit, and the measurement circuit. The second circuit board is the DSP development platform eZdsp TMS320F28335, which handles the controlling. The controller was implemented in the DSP by using C programming language.

The circuit diagram of the power-stage is presented for both of the converters in Appendix B. There are differences in the damping network, inductor and input capacitor as discussed earlier. Also the circuit diagram of the measurement circuit for the input voltage is presented, which is basically a differential amplifier with a low-pass filter. The purpose of this circuit is to scale the input voltage to a level acceptable for the AD converter and to remove high-frequency disturbances. The last circuit diagram in Appendix B includes the driver circuit and the voltage regulator of the measurement circuit.

The control signal of the PWM output of the DSP is connected to the input of the driver circuit and the output of the measurement circuit is connected to the AD converter of the DSP. The supply voltage of 10V for the driver is provided from the laboratory power supply.

Photograph of the converter prototypes is presented in Fig. 5.1. The upper converter is Converter CM and the lower is Converter NM. As it is clearly visible, the inductor, connectors and the heat sink of the MOSFET are heavier when the conventional design method is used. It should be noted that only the other of the two similar inductors is visible in Fig. 5.1, the other one is under the PCB.

a)

b)

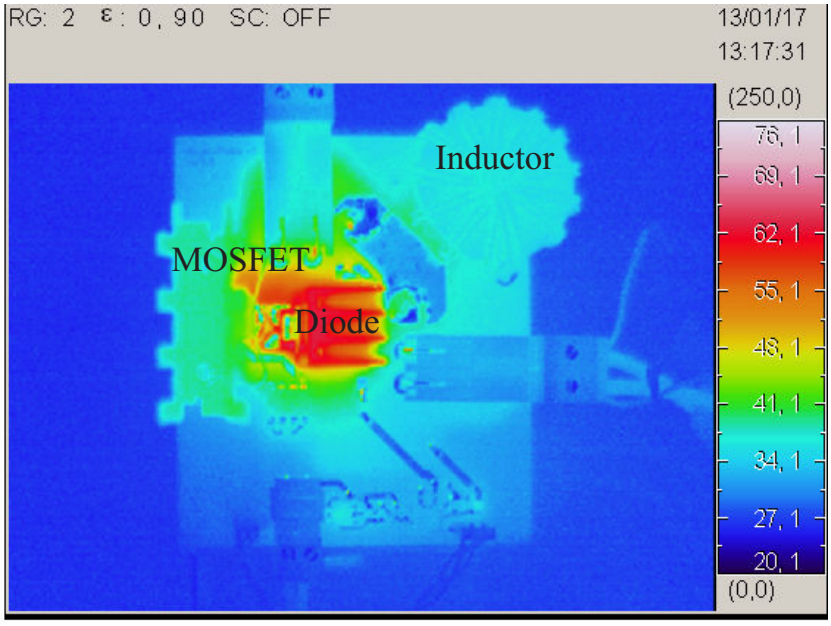
Figure 5.1: Prototypes: a) Converter CM, and b) Converter NM.

As the difference in the size of these two converters is remarkable, it is clear that the second design method might be desirable in the applications, where the cost and size are determining factors in design.

5.2 Thermal Distribution

Temperature distribution of the converters was measured at three operating points by using NEC TH7800 Thermo Tracer. It was first waited that the converter under measurement reached its final temperature before the thermal image was taken. The thermal distribution of the prototype converters is presented in Fig. 5.2 when they operate at the MPP in the STC. The upper image corresponds to Converter CM and the lower image corresponds to Converter NM.

a)



b)

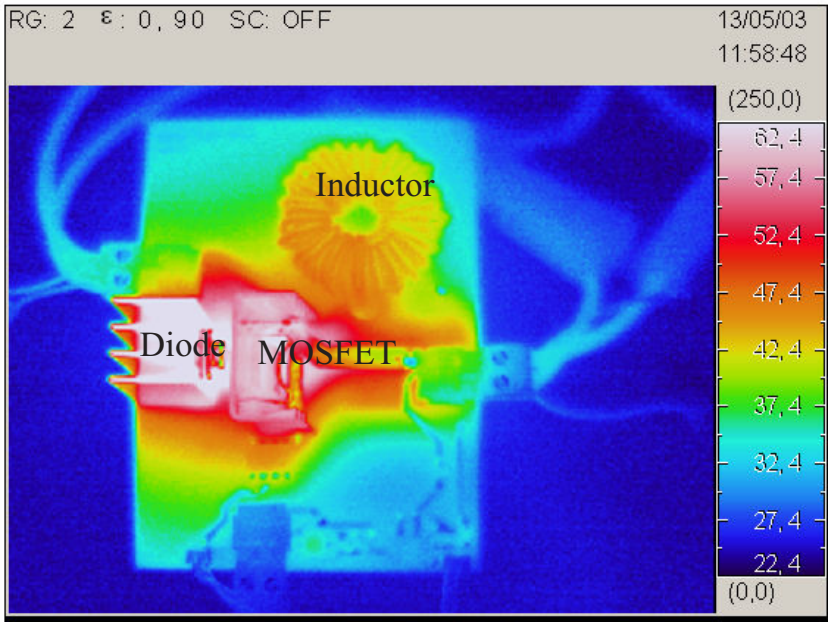


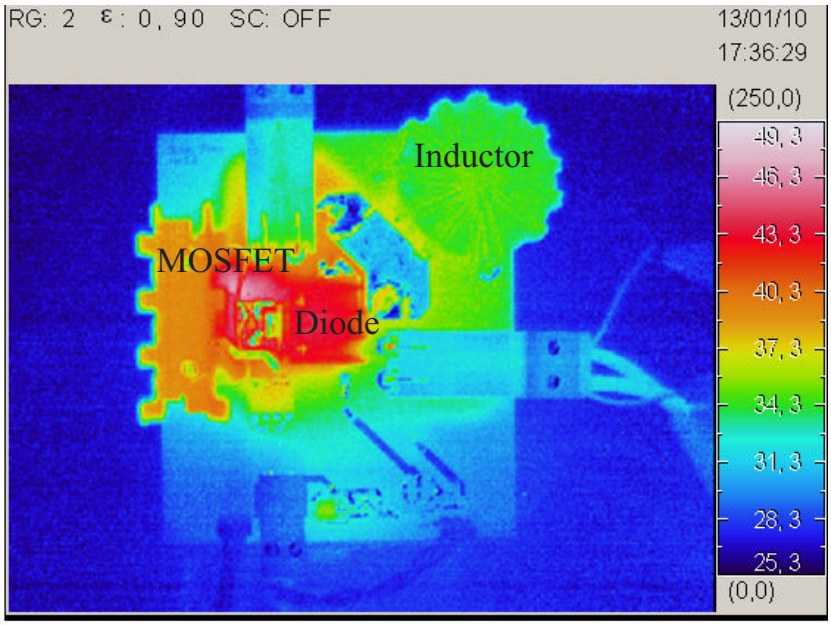
Figure 5.2: Thermal distribution of the prototype converters at the MPP in the STC: a) Converter CM and b) Converter NM.

As it is shown in Fig. 5.2, the temperature distribution between the semiconductors is more even in the lower converter, whereas the MOSFET is running quite cool in the upper converter. Still, the temperature of the diode is the same in both of the converters predicting equal lifetime expectancy. This result was expected according to Section 4.3. It is worth mentioning that the ambient temperature was lower during the measurements than the value used in the calculations. However, absolute temperature values are not relevant, because we are interested in the comparison of the temperatures between these two converters.

The temperature distributions of the prototype converters is presented in Fig. 5.3 when they operate in the CC region in the STC. The order of the converters is the

same as in Fig. 5.2.

a)



b)

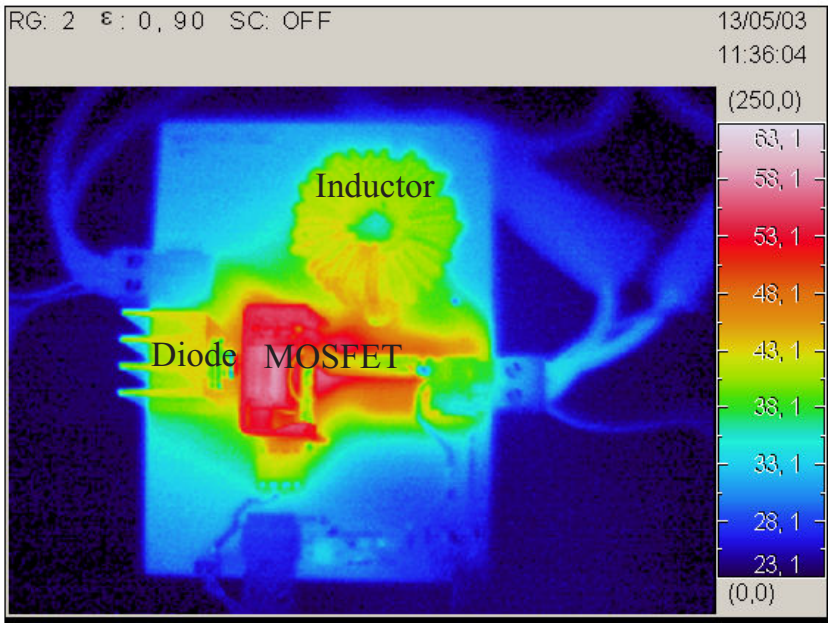


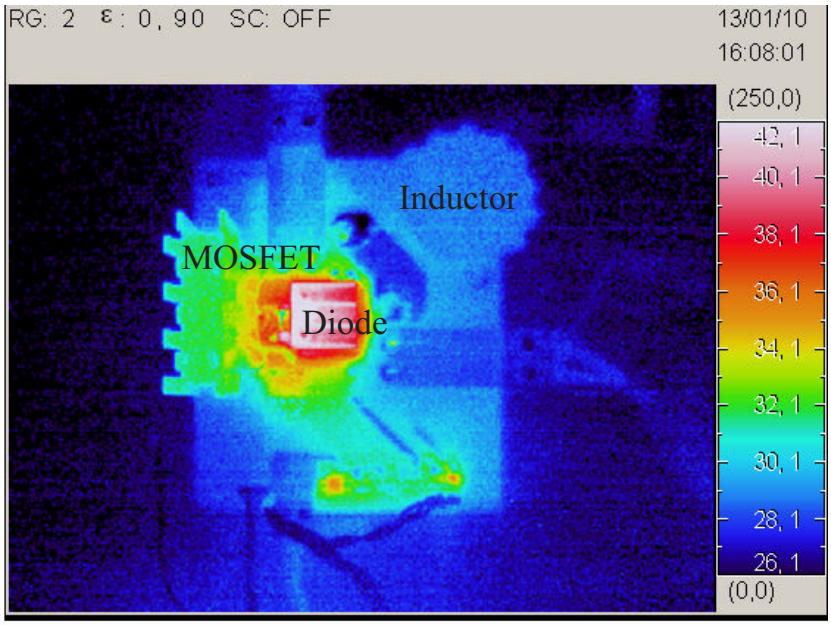
Figure 5.3: Thermal distribution of the prototype converters in the CC region in the STC: a) Converter CM and b) Converter NM.

As it is shown in Fig. 5.3, the temperature distribution between the semiconductors is more even in the upper converter. This was expected, because the semiconductor power losses of the upper converter were calculated at this operating point and the calculated values were used in the heat sink selection. The temperature distribution of the lower converter is more uneven, but the most important thing is that the temperature of the MOSFET is not higher than the temperature of the diode at the MPP. This implies that the MOSFET is not overheated in the lower converter even if its temperature is higher than in the upper converter.

As it is visible in Figs. 5.2 and 5.3, the maximum power loss of the MOSFET occurs

at the minimum input voltage, and the maximum power loss of the diode occurs at the MPP. This verifies the results that were presented in Section 4.3. The thermal image of the prototype converters was also taken in the CV region in the STC and is presented in Fig. 5.4. The order of the converters is the same as in Fig. 5.2.

a)



b)

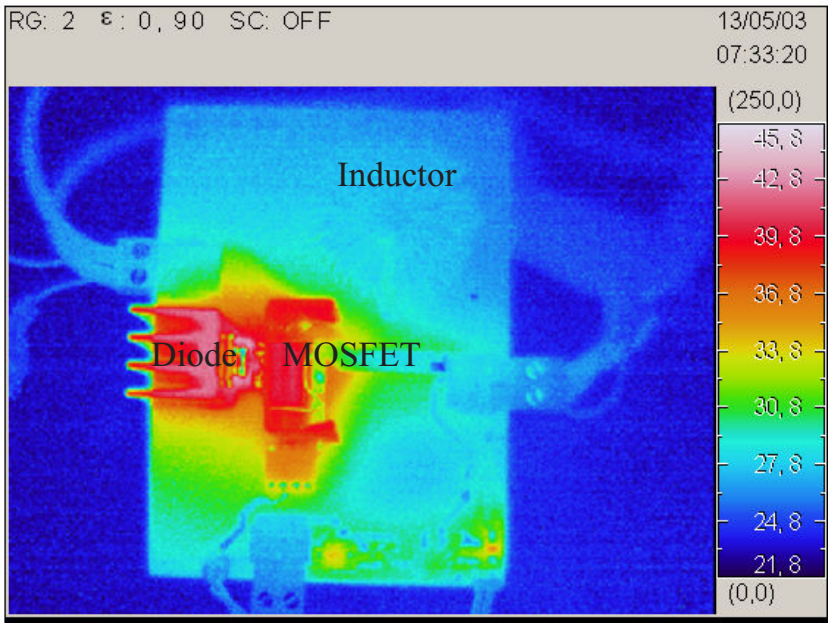


Figure 5.4: Thermal distribution of the prototype converters in the CV region in the STC: a) Converter CM and b) Converter NM.

As it is shown in Fig. 5.4, the temperature levels in both of the converters are low, which is caused by the low output power and current of the PV module in the CV region. This is also consistent with the discussion in Section 4.3. The overload protection of the converter connected to PV module can be made my moving the operating point away from the MPP. According to Fig. 5.3 and Fig. 5.4, the operating point should be moved towards the CV region instead of the CC region for more efficient cooling.

As a summary, it can be said that the converter, which is designed by using the conventional design method, is oversized, because the MOSFET and inductor are running cool, whereas in the converter, which is designed by using the new design method the MOSFET is as hot as the diode.

5.3 Input Voltage Ripple

The input voltage ripple of the converters was measured at the MPP in the STC by using LeCroy104MXi oscilloscope. The measured input voltages are presented in Figs. 5.5 and 5.6. As it is shown, the amplitude of the ripple component at the input voltage is approximately equal, which verifies that the converters operate similarly from this point of view and thus, the comparison is reasonable. The peak-to-peak value of the voltage ripple is approximately 250mV. This value was used when the effect of the voltage ripple on power output of the PV module was calculated in Section 4.5.

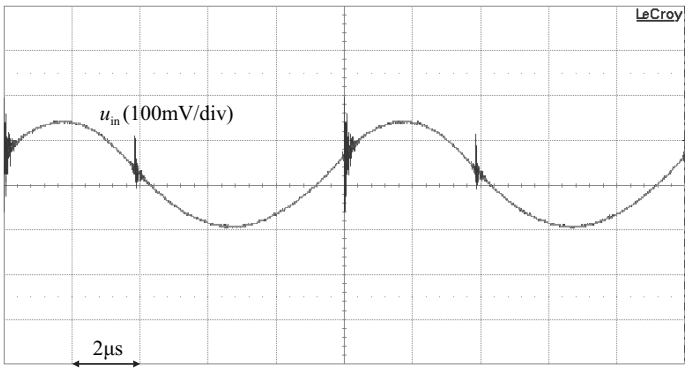


Figure 5.5: The input voltage ripple of Converter CM.

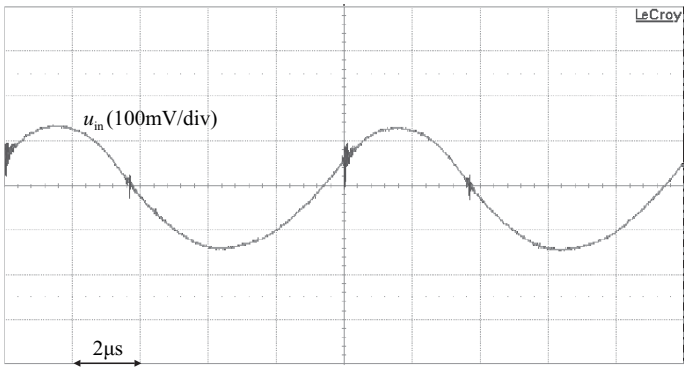


Figure 5.6: The input voltage ripple of Converter NM.

5.4 Frequency Response Measurements

The frequency responses of the converter prototypes were measured by using the frequency response analyzer Model 3120 of Venable Instruments. Every open-loop and closed-loop transfer functions were measured at three operating points in order to verify the converter model and the control design. Also the impedance of the ceramic

capacitor was measured to determine its ESR and capacitance values for the model at these operating points. The output impedance of the SAS was also measured and its effect on the model was taken into account. The final tuning of the model parameters was made so that all of the predicted and measured transfer functions matched as well as possible.

As it is shown in Figs. 5.7 and 5.8, the control to input transfer function of the converters are quite similar with phase starting from 180 degrees and gain from 30 decibels. The resonance peak is smooth in the CC region because of the added damping circuit as explained in Section 4.5. The predicted transfer functions (dots) correlate well with the measurements in the CC region (solid) and in the CV region (dotted).

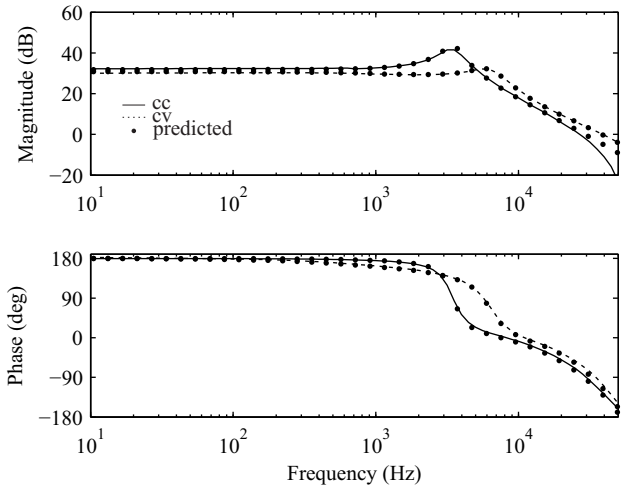


Figure 5.7: Control to input transfer function of Converter CM.

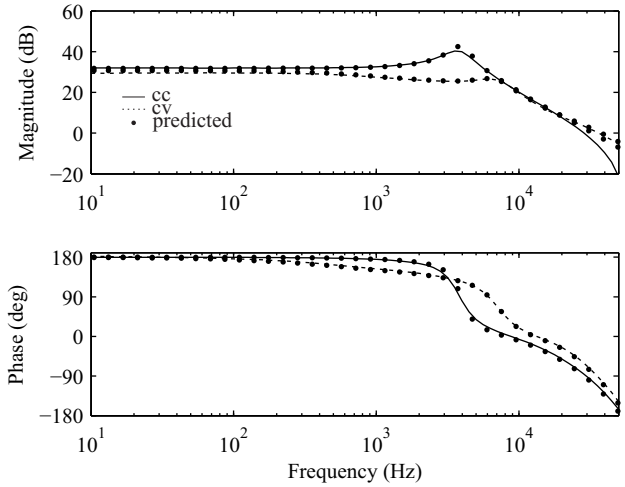


Figure 5.8: Control to input transfer function of Converter NM.

The input-voltage loop gain L_{in} can be solved from (3.9) by taking into account that the sensing gain is set to unity in the program of the DSP. Thus, L_{in} can be calculated

by using the measured reference-to-input voltage transfer function G_{ri} as follows

$$L_{\mathrm{in}} = -\frac{G_{\mathrm{ri}}}{1 - G_{\mathrm{ri}}}. \tag{5.1}$$

The loop-gains of the converters are presented in Figs. 5.9 and 5.10. The predicted loop-gains (dots) correlate well with the measurements in the CC region (solid) and in the CV region (dotted). The gain and phase margins are the same in both of the converters as predicted. The gain margin is a bit smaller in Fig. 5.10, which was plotted with the fitted model compared to the gain margin in Fig. 4.4, which was plotted with inaccurate model. However, both of the margins are sufficient for stable operation. The control bandwidth is approximately 300Hz in both of the converters.

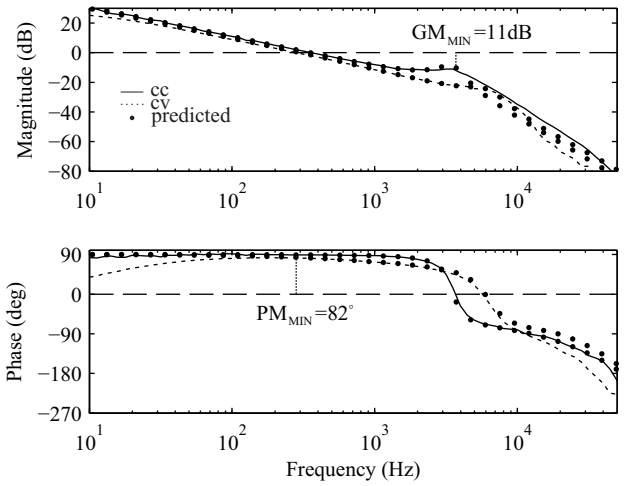


Figure 5.9: The loop gain of Converter CM.

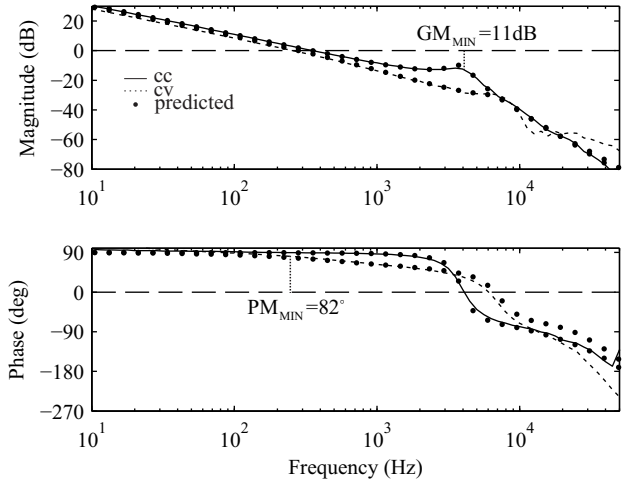


Figure 5.10: The loop gain of Converter NM.

The closed-loop reverse voltage transfer ratio $T_{\mathrm{oi\text{-}c}}$ is presented in Figs. 5.11 and

5.12. The predicted transfer functions (dots) correlate well with the measurements in the CC region (solid) and in the CV region (dotted). As it is shown, the magnitude at 100Hz is -13dB in both of the converters in the CC region, which verifies the similarity of the attenuation behavior of the converters. It is also visible that the magnitude of $T_{\text{oi-c}}$ is usually lower than -13dB at 100Hz, because the operation point is varying between the lowest and highest input voltage. The attenuation is most important in the MPP, because the ripple at the PV module voltage would cause highest losses.

According to the input-voltage ripple and frequency response measurements, it can be said that both of the converters operate electrically similarly in terms of the given quantities. Because Converter NM offers the same performance as Converter CM with a lower inductor core size and smaller capacitors, converter NM is more optimal. Thus, the measurements verify the claims that are presented earlier in this thesis.

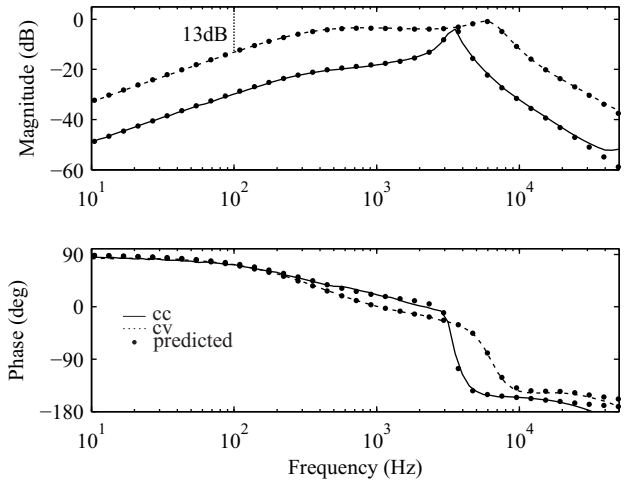


Figure 5.11: Closed-loop reverse voltage transfer ratio $T_{\text{oi-c}}$ of Converter CM.

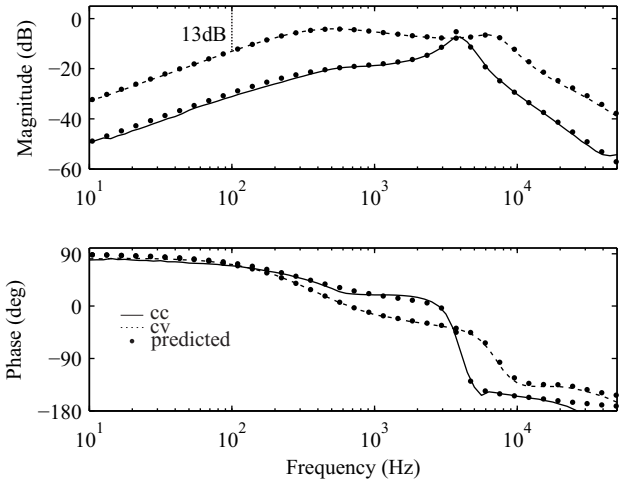


Figure 5.12: Closed-loop reverse voltage transfer ratio $T_{\text{oi-c}}$ of Converter NM.

6. CONCLUSIONS

Two differently designed boost-power-stage converters were implemented and compared to each other in this thesis. The first converter was designed by using the conventional method and the second converter was designed by using the new method taking into account the maximum values of the PV module output.

In the conventional design method, it was assumed that the maximum power loss of the diode and power switch would occur in the minimum input voltage condition. However, it was theoretically explained and verified by the measurements that the maximum power loss of the power switch occurs in the minimum input voltage condition, whereas the maximum power loss of the diode occurs when the PV module is at the maximum power point.

The converters were designed in such a way that both have the same amount of switching frequency input-voltage ripple and equal ability to prevent low frequency output voltage ripple from affecting the input voltage. Despite of this electrical similarity, which was also verified by the measurements, the converter that was designed by using the second design method has smaller core size, less capacitance in the input and damping capacitors as well as has smaller heat sink of MOSFET. Thus, it is possible to obtain significant cost savings if the second design method is used.

In the new design method, it was taken into account that the output power of the PV module is momentarily high due to peaks in solar irradiance. This way it can be ensured that the inductor will not saturate in any circumstances. If the inductor saturation and semiconductor overheating can be prevented by some kind of protection method, it would be possible to undersize the components and the difference between the presented design methods would be even more significant. However, this requires more research on different protection methods and thus might be a possible topic in the future.

The results presented in this thesis are most valuable for a manufacturer, who delivers both the PV generator and the power electronic devices, because the properties of a PV generator are known when the converter or inverter is designed. On the other hand, it might be interesting for a manufacturer, who produces only PV inverters to know how much oversizing the conventional sizing method causes. Even if the converter prototypes were designed for a PVG consisting only one PV module, the results are applicable also for a string of modules. Only the voltages are scaled but the current remains the same.

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A. IMPEDANCE MEASUREMENT OF THE INDUCTORS

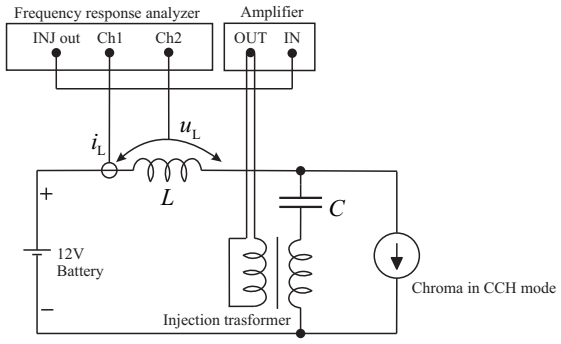

Figure A.1: Inductor impedance measurement setup.

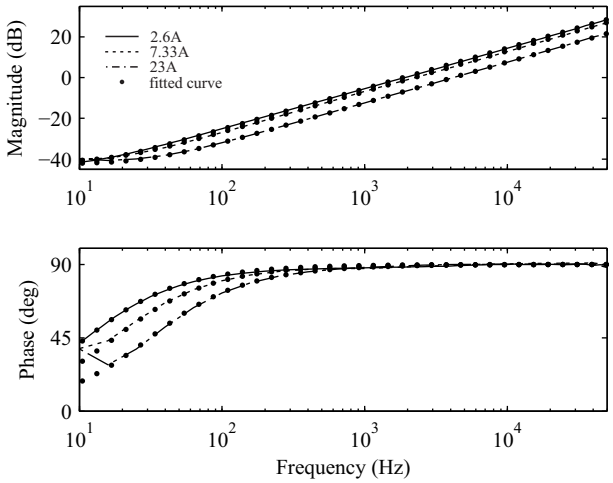

Figure A.2: Measured impedances of the 43-μH inductor for different bias currents with fitted curves.

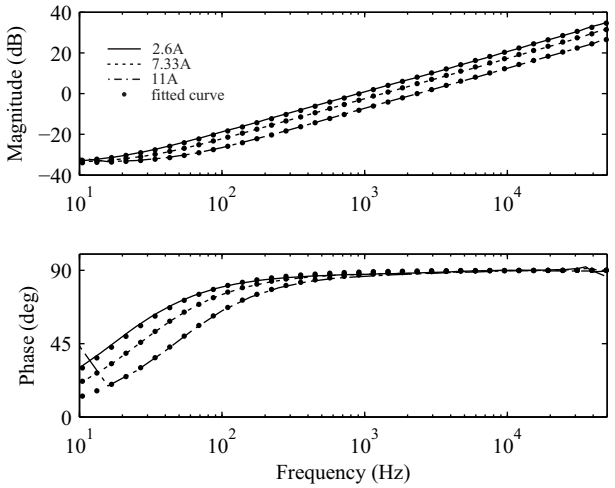

Figure A.3: Measured impedances of the 89-μH inductor for different bias currents with fitted curves.

B. SCHEMATICS OF THE PROTOTYPE CONVERTERS

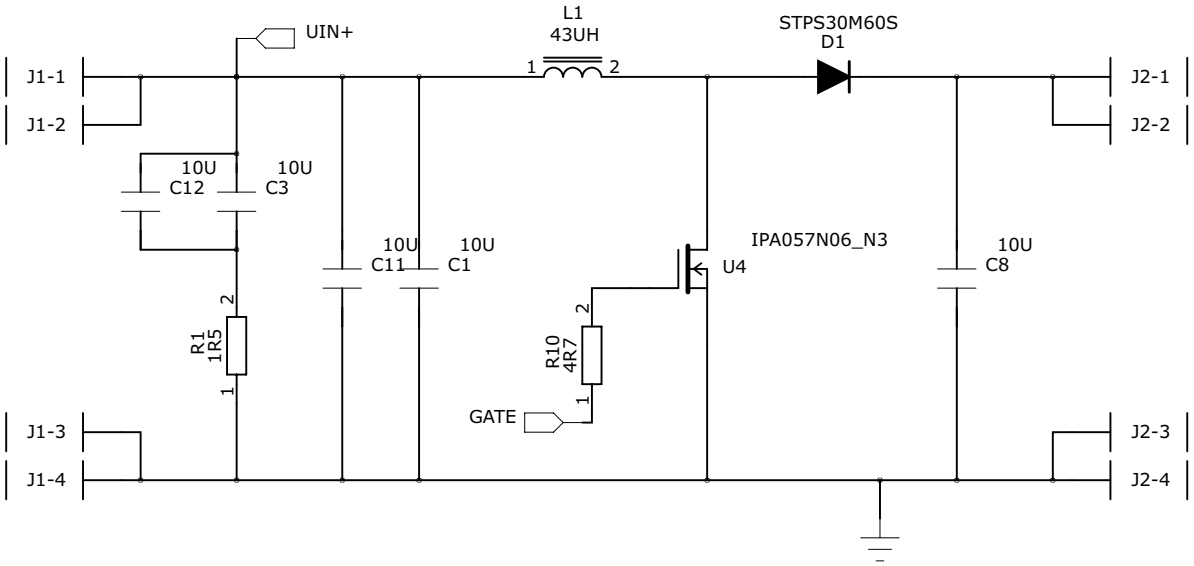

Figure B.1: Power-stage of Converter CM.

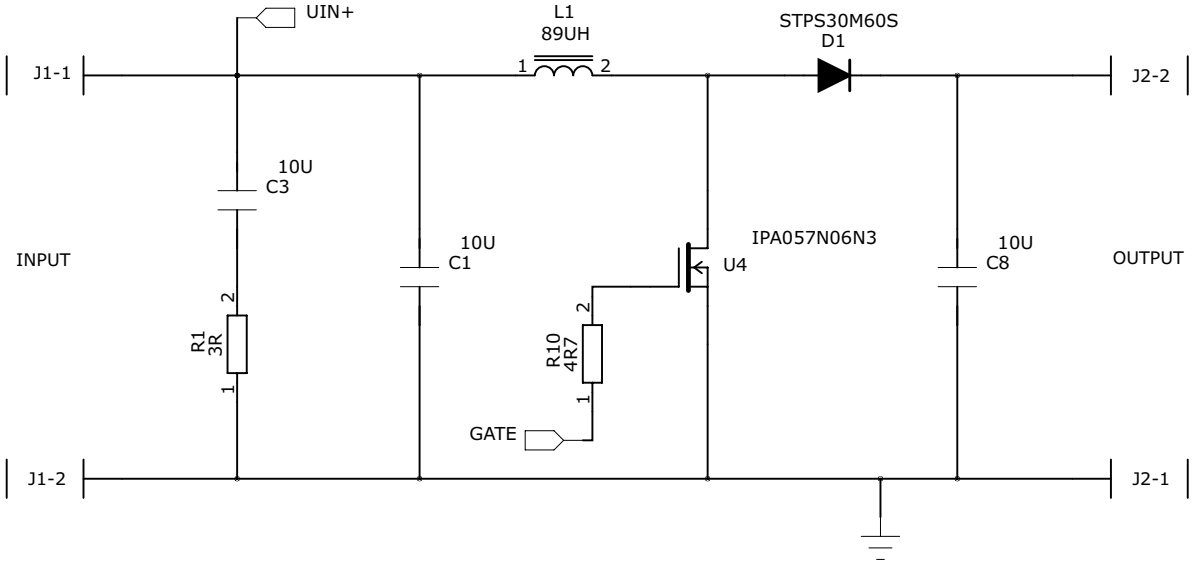

Figure B.2: Power-stage of Converter NM.

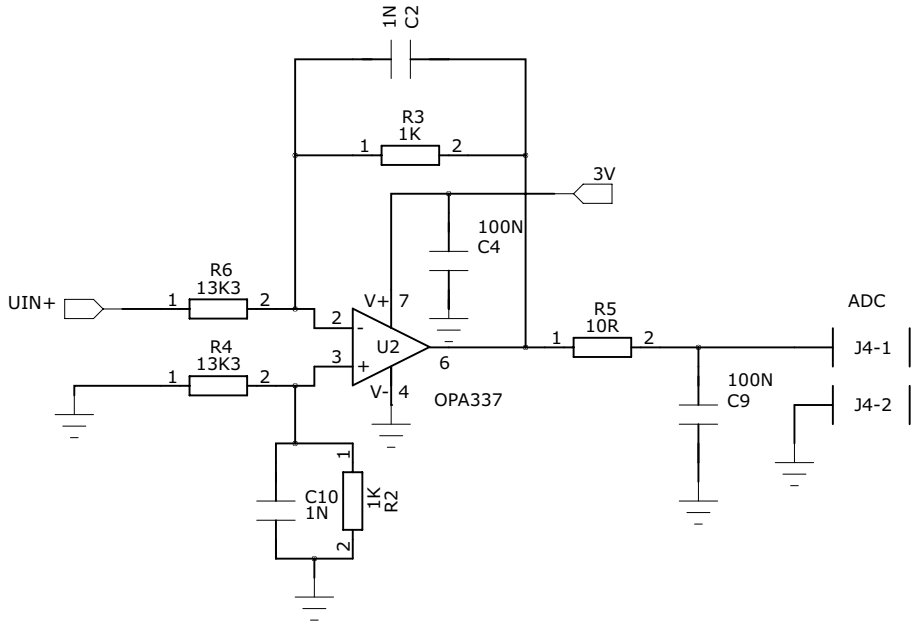

Figure B.3: Measurement circuit for the input voltage.

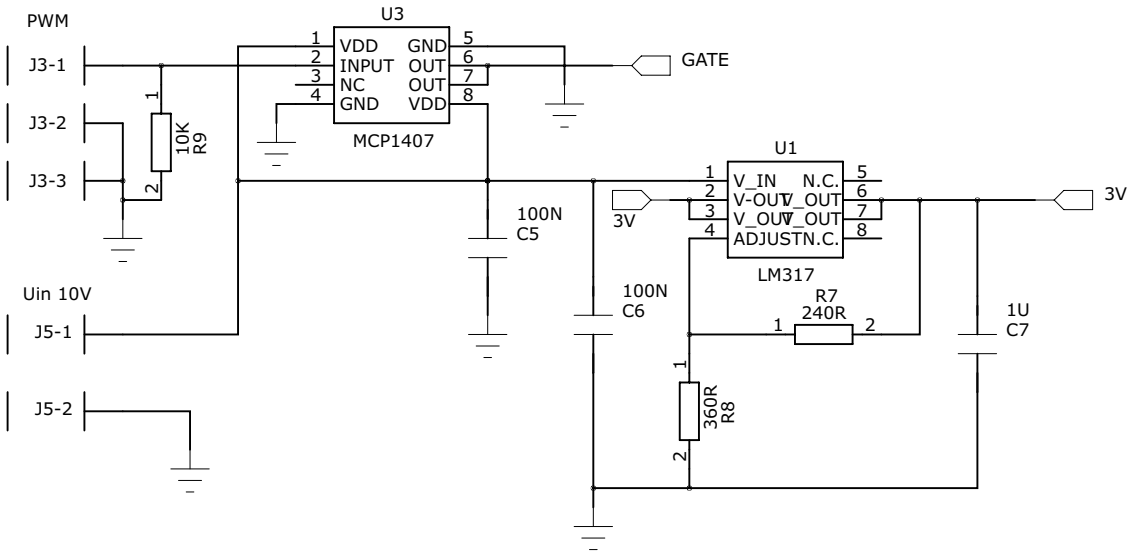

Figure B.4: Driver circuit and the voltage regulator.